Mono FSTN Display Module

Product Specification
Part No. YMS-12864-18AEGFDGL
128 x 64 FSTN Display

For more information, please visit www.andersdx.com
or email info@andersdx.com

Version 1.0

Interfaces to Inspire

SPECIFICATIONS FOR
LIQUID CRYSTAL DISPLAY MODULE

MODEL NO.: YMS12864-18AEGFDGL DATE: SEP.02.2015

Approved	Checked	Department

CUSTOMER:

MODEL NO.: DATE:

Approved	Checked	Department

REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	SEP.02.2015	New Creation	ALL	

LIST

Ⅰ. General Specifications

1.Features

Item	Contents	Unit
Drive Method	1/64 Duty ,1/9 Bias	/
Operating voltage	3.3	V
Viewing direction	6:00	O' Clock
Operating Temperature	-20~70	℃
Storage Temperature	-30~85	℃
Display type	FSTN mode, Transflective, Positive type display	/
Module Size	72.0 *52.0	mm
View Area	66.4*39.4	mm

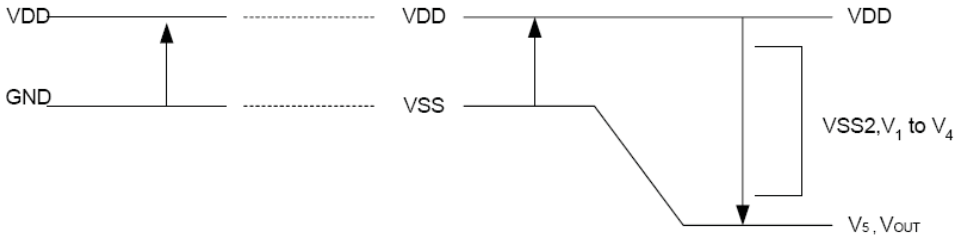
2.Pin Connections:

Pin No.	Symbol	Function
1	P/S	This is the parallel data input/serial data input switch terminal
2	C86	This is the MPU interface switch terminal
3-7	V5-V1	This is a multi-level power supply for the liquid crystal drive VDD≥V1≥V2≥V3≥V4≥V5
8	CAP2+	DC/DC voltage converter capacitor 2 positive connection
9	CAP2-	DC/DC voltage converter capacitor 2 negative connection
10	CAP1-	DC/DC voltage converter capacitor 1 negative connection
11	CAP1+	DC/DC voltage converter capacitor 1 positive connection
12	CAP3-	DC/DC voltage converter capacitor 3 negative connection
13	VOUT	DC/DC converter output
14	VSS	Ground
15	VDD	Power supply for logic
16-23	D7-D0	Data bit

24	/RD(E)	Signal to select read and write
25	/WR(R/W)	Signal to select read and write
26	A0	Control/data select signal
27	/RES	Reset signal
28	/CS1	Chip select signal

3. Absolute Maximum Ratings

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		VDD	-0.3 to + 7.0	V
Power supply voltage (2) (VDD standard)	With Triple step-up	VSS2	-7.0 to +0.3 -4.0 to +0.3	V
	With Quad step-up		-3.0 to +0.3	
Power supply voltage (3) (VDD standard)		V_5, V_{OUT}	-12.0 to +0.3	V
Power supply voltage (4) (VDD standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	-0.3 to VDD +0.3	V
Output voltage		V_O	-0.3 to VDD +0.3	V



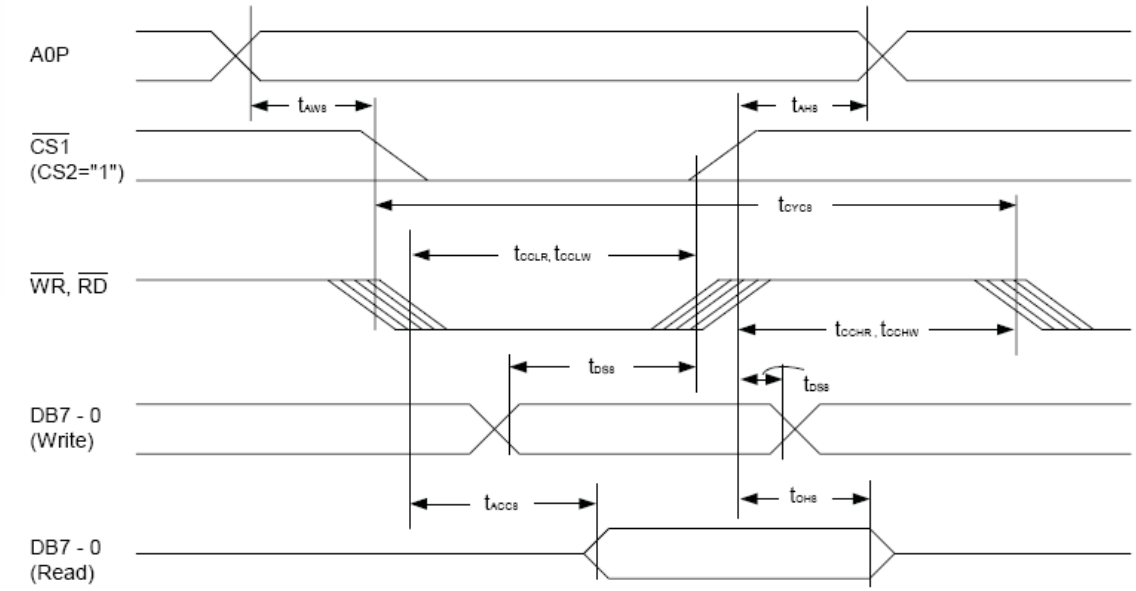
System (MPU) side SPLC501C chip side

Notes and Cautions:

1. The VSS2, V_1 to V_5 and VOUT are relative to the VDD = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that VDD≧V_1≧V_2≧V_3≧V_4≧V_5.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

4.Timing Characteristics:

System bus read/write characteristics 1 (For the 8080 Series MPU)



(VDD = 2.7V to 4.5V, T_A = 25℃)

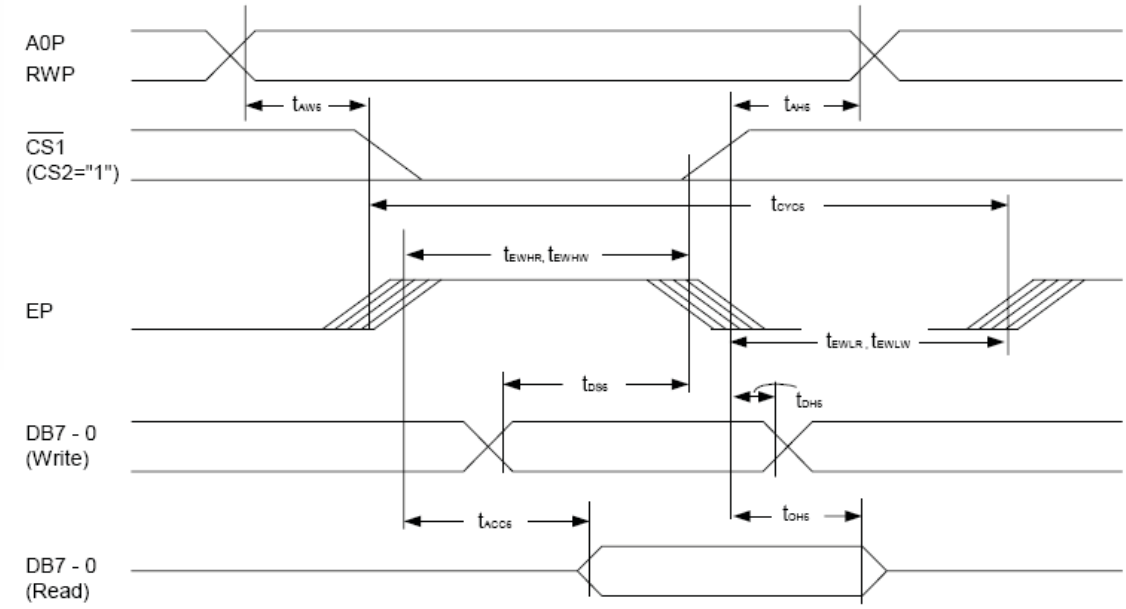
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		300	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	-	ns
Data setup time	DB7 - 0	t_{DS8}		40	-	ns
Address hold time		t_{DH8}		15	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	140	ns
Output disable time		t_{OH8}		10	100	ns

Note1: The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being 'L' ($\overline{CS2}$ = 'H') and $\overline{WR}$ and $\overline{RD}$ being at the 'L' level.

System bus read/write characteristics 2 (6800 series MPU)



(VDD = 2.7V to 4.5V, T_A = 25℃)

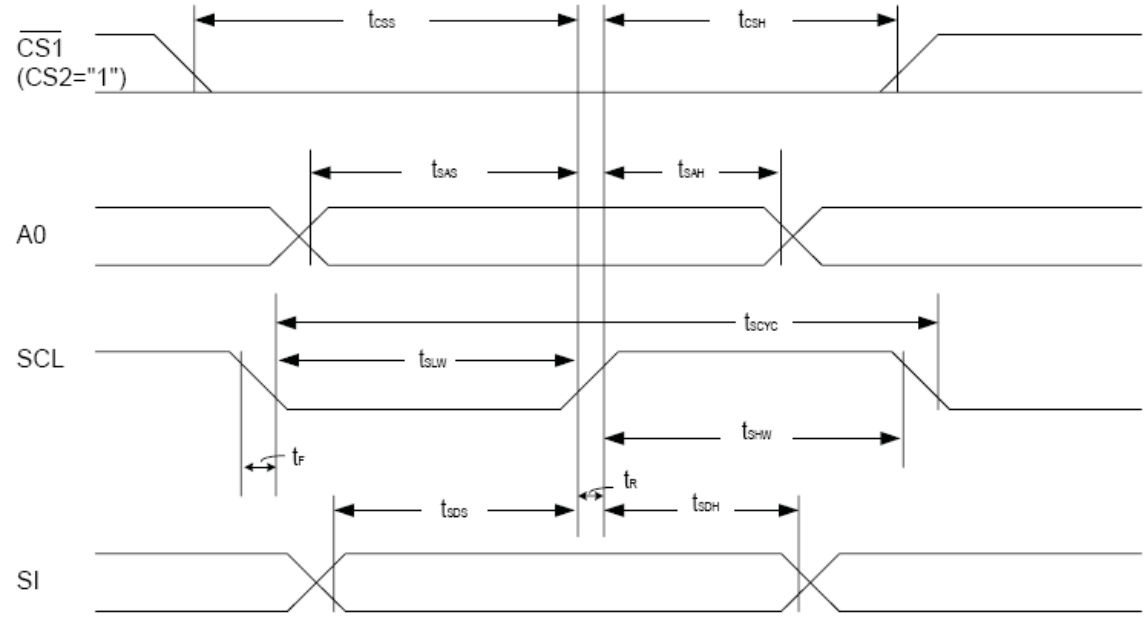
Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		300	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	40	-	ns
Data hold time			t_{DH6}		15	-	ns
Access time			t_{ACC6}		-	140	ns
Output disable time			t_{OH6}		10	100	ns
Enable H pulse time	Read	EP	t_{EWHR}		120	-	ns
	Write		t_{EWHW}		60	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		60	-	ns
	Write		t_{EWLW}		60	-	ns

Note1: The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being 'L' (CS2 = 'H') and EP.

The serial interface



(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	-	250	-	ns
SCL 'H' pulse width		t_{SHW}	-	100	-	ns
SCL 'L' pulse width		t_{SLW}	-	100	-	ns
Address setup time	A0P	t_{SAS}	-	150	-	ns
Address hold time		t_{SAH}	-	150	-	ns
Data setup time	SI	t_{SDS}	-	100	-	ns
Data hold time		t_{SDH}	-	100	-	ns
CS-SCL time	CS	t_{CSS}	-	150	-	ns
		t_{CSH}	-	150	-	ns

Note1: The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
Note2: All timing is specified using 20% and 80% of VDD as the standard.

Ⅱ.The Characteristics and The Reliability Test

1. Electro-Optic Characteristics:

Measuring Condition: TEMP=(23±3)℃, HUM= (55±10)%RH

NO.	Item		Symbol	Min	Type	Max	Unit
1	Operating Voltage		Vlcd	9.5	9.7	9.9	V
2	Operating Frequency		F		64		Hz
3	Response Time	Rising Time	Tr		60		mS
		Decay Time	Td		316		
4	Contrast Ratio		CR	3			
5	Viewing Angle (CR≥2)	12H Φ=90°	θ 1		45		deg
		6H Φ=270°	θ 2		55		
		3H Φ=0°	θ 3		50		
		9H Φ=180°	θ 4		50		

2. Characteristics of backlight (LED unit)

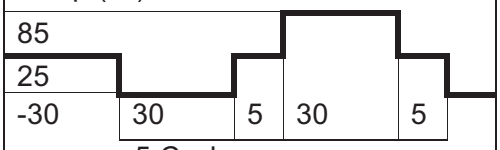
Color:White

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	Vf	2.85	3.2	3.5	V	--
Forward Current	If	--	90	120	mA	Vf= 3.2V
Power Dissipation	Pd	--	0.288	--	W	If= 90 mA
Reverse Voltage	Vr	--	--	5.0	V	VR=5.0V Each chip
Reverse Current	Ir	--	--	10	μA	
Luminous Intensity	Lv	--	TBD	--	cd/m^2	If= 90 mA
Luminous Uniformity	ΔLv	70	--	--	%	If= 90 mA
Chromaticity coordinate	X	X=0.270	--	X=0.320		If=20mA Ta=25° C Each chip
	Y	Y=0.270	--	Y=0.320		

WARNING:

A BACKLIGHT IS A KIND OF CURRENT DEVICE,IT MUST CONNECT WITH A RESISTOR FOR LIMITING CURRENT ,OR IT WILL BE DAMAGED.

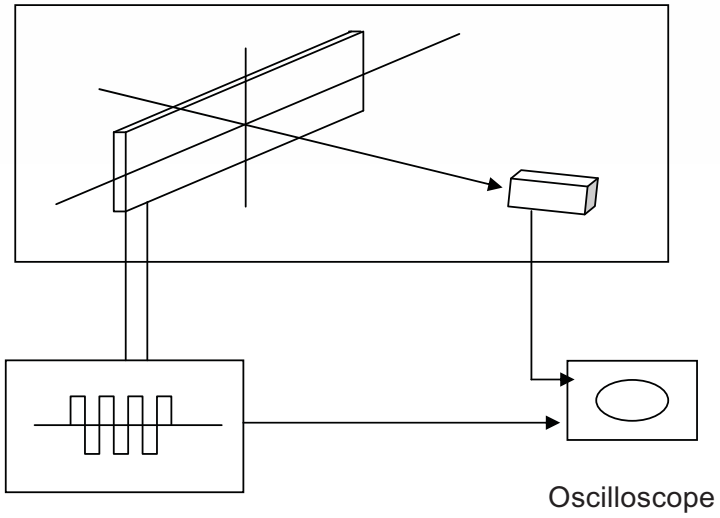
3.Reliability Test

No	Items	Test Condition	Test Result
1	High Temp Storage	Temp:85±2℃ Time:96h Restore:24h	Passed
2	Low Temp Storage	Temp:-30±3℃ Time:96h Restore:24h	Passed
3	HIGH TEMP OPERATING	Temp:70±2℃ Vop:3.3V Time:24h Restore:24h	Passed
4	LOW TEMP OPERATING	Temp:-20±3℃ Vop:3.3V Time:24h Restore:24h	Passed
5	High Temp High Hum Storage	Temp:40±2℃ Hum:90%Rh Time:96h Restore:24h	Passed
6	Thermal Shock	Temp:(℃)  5 Cycles Restore:24h	Passed

Ⅲ.The LCD Measuring Method and Equipment

1. Threshold Voltage and Response Time Measuring

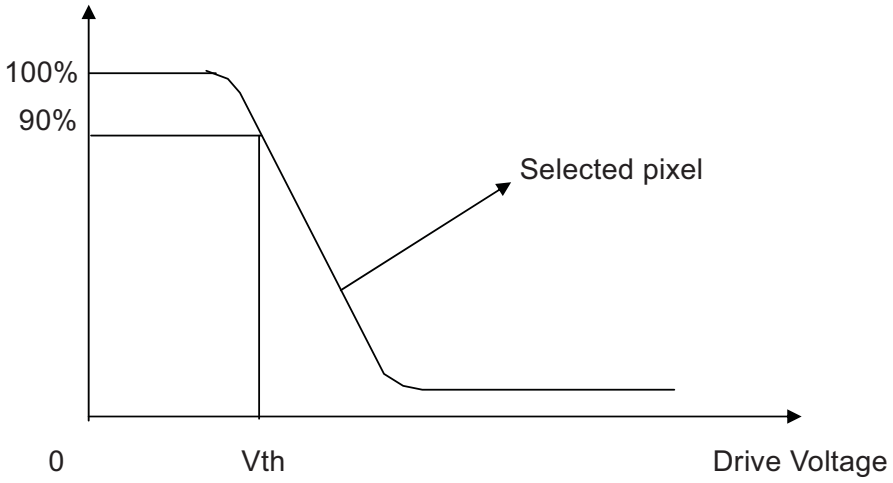
(1) Equipment



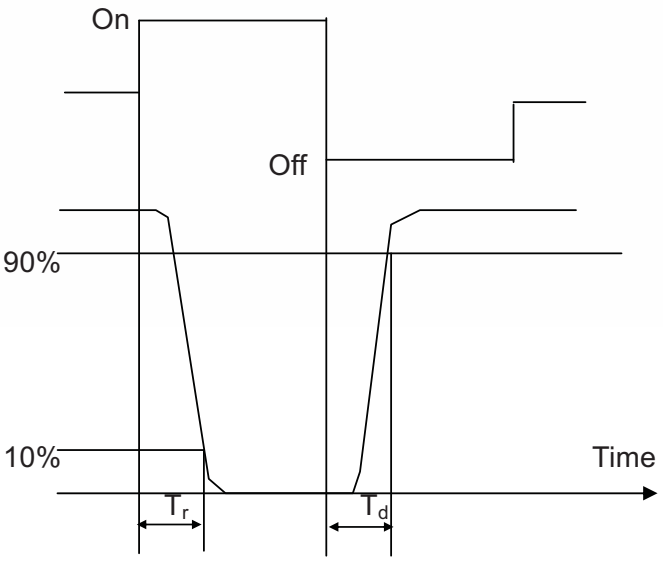
(2) Definition

A. Threshold Voltage (Vth)

Brightness

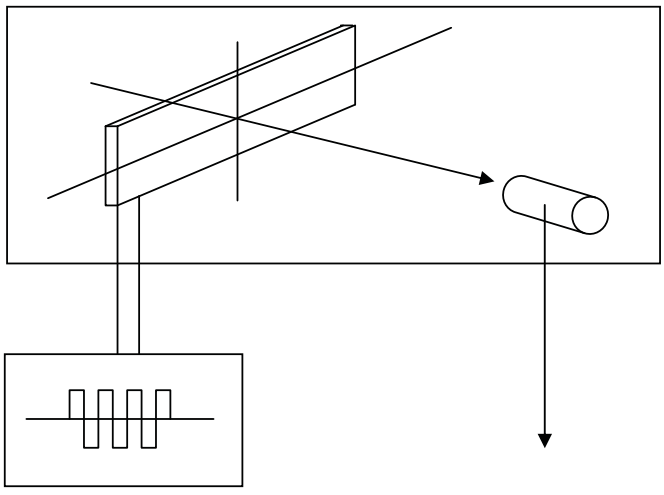


B. Response Time



2. Contrast Measuring

(1) Equipment

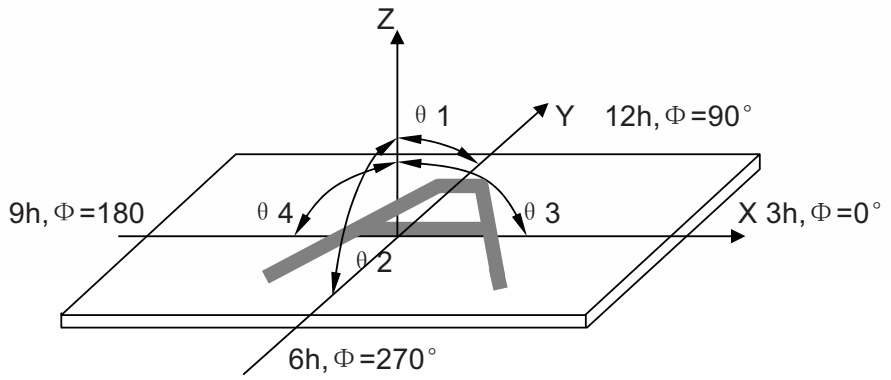


Spectrophotometer

Waveform Generator

(2)Definition:

A.Viewing Angle:



B. Contrast Ratio (Positive)

$$CR = \frac{\text{Brightness of non-selected pixel}}{\text{Brightness of selected pixel}}$$

3. Reliability Test:

Equipment : TENNY

Ⅳ.Standard Specifications for Product Quality

1.Warranty time: one year

2. MTBF

More than 50,000 hours.

3. Manner of test:：

1.1 The test must be under 40W fluorescent light, and the distance of view must be at 30cm.

1.2 The test direction is based on around -10°- 30° of Vertical line.

4.Quality specification

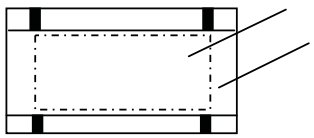
It shall be based on GB2828-87, Apply level II, Normal inspection by single sampling.

	IETM	CHECK LEVEL	AQL
MAJOR (MA)	1.LIQUID CRYSTAL LEAKAGE 2.WRONG POLARIZER 3.OUTSIDE DIMENSION 4.SEGMENT MISSING 5.SEGMENT SHORT	II	0.25
MINOR (MI)	1.BLACK SPOTS OR WHITE SPOTS. 2.FOREIGN SUBSTANCE, 3.WHITE SPOTS, 4.PINHOLE,SEGMENT 5.DEFORMATION SCRATCHS(GLASS & POLARIZER), 6.SEGMENT DEFECT, 7.AIR BUBBLES BETWEEN GLASS & POLARIZER, 8.COLOR VARIATION,GLASS CHIPS, 9.OTHER VISUAL DEFECTS.	II	1.0

5. Definition of area:

3.1 Ⅰ area: viewing area

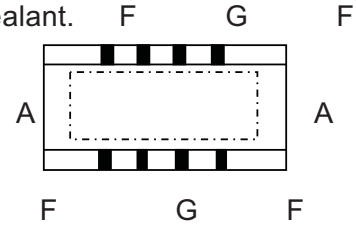
Ⅱ area: outside viewing area



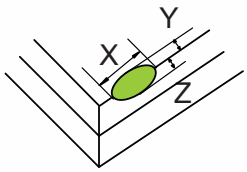
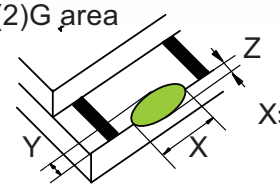
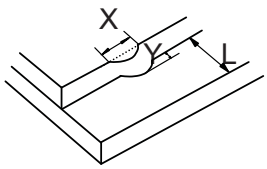
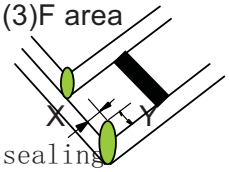
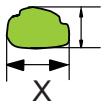
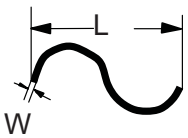
3.2 A area: The glass area outside sealant.

G area: Electrode pad area.

F area: Without electrode pad area.

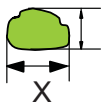
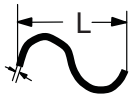
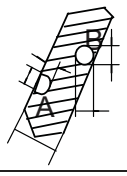
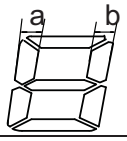
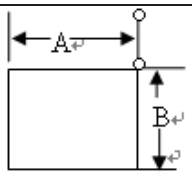


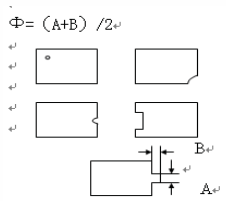
6.Standard of appearance test: (unit: mm)

№	Items	Criterion	Checking manner
1	Substrate crack X: defect Length Y: defect Width Z: defect Depth T: glass Thickness N: defect QTY L:Connector Width	(1) A area  X≤3.0 Y：Don’t allowed hurt sealing Z≥T/2 N≤3 X≤5.0 Y：Don’t allowed hurt sealing Z≤T/2 N≤3 X≤1.0 Y≤0.5 Z≤T/3 No check (2)G area  X≤3.0 Y≤0.5 Z≤T/2 N≤2  X≤total length Y≤1/4L N≤1 Over the drawing tolerance is not allowed (3)F area  X≤2.0 Y≤3 Z≤T N≤3 Don’t allowed hurt sealing	checking with eyes
2	Black spot white spot D=(X+Y)/2 Line	(1)  0.2<D≤0.25 N≤1 0.1<D≤0.2 N≤3 D≤0.1 No check (2)  L≤2.0 W≤0.03 N≤2 L≤1.0 W≤0.05 N≤1	Checking on the table with light and polarizer and checking with eyes directly.

№	Items	Criterion	Checking manner
3	Polarizer Bubble	D≤0.15 No check 0.15<D≤0.4 N≤2	Checking on the table with light and polarizer, and checking with eyes directly
4	Rainbow Color	Allow tiny rainbow Allow 5% color contrast or accord limitative sample	Checking on the table with light and polarizer, And checking with eyes directly
5	END Seal	1. Dimension accord design require 2. Inject depth（d）：1/5D≤d≤D （D：seal design depth）	Checking with eyes
6	Polarizer or pad appearance	No dirty	Checking with eyes

7 Standard of display test

№	Items	Criterion	Checking manner
1	Black spot white spot D=(X+Y)/2 Line	(1)  0.2<D≤0.25 N≤1 0.1<D≤0.2 N≤3 D≤0.1 No check (2)  L≤2.0 W≤0.03 N≤2 L≤1.0 W≤0.05 N≤1	Checking at the display state
2	Pin hole D=(A+B)/2 W: segment width	 W≤0.4 D≤0.20 And D≤1/2W N≤1 W>0.4 D≤0.25 And D≤1/3W N≤2 D≤0.05 No check	Checking at the display state
3	Different width of segment	 |a-b|<0.25 or |a-b|≤1/4W No check	Checking at the display state
4	Different width		A：distortion≤10% B：distortion≤10% Superfluous Electrode lines display is not allowed

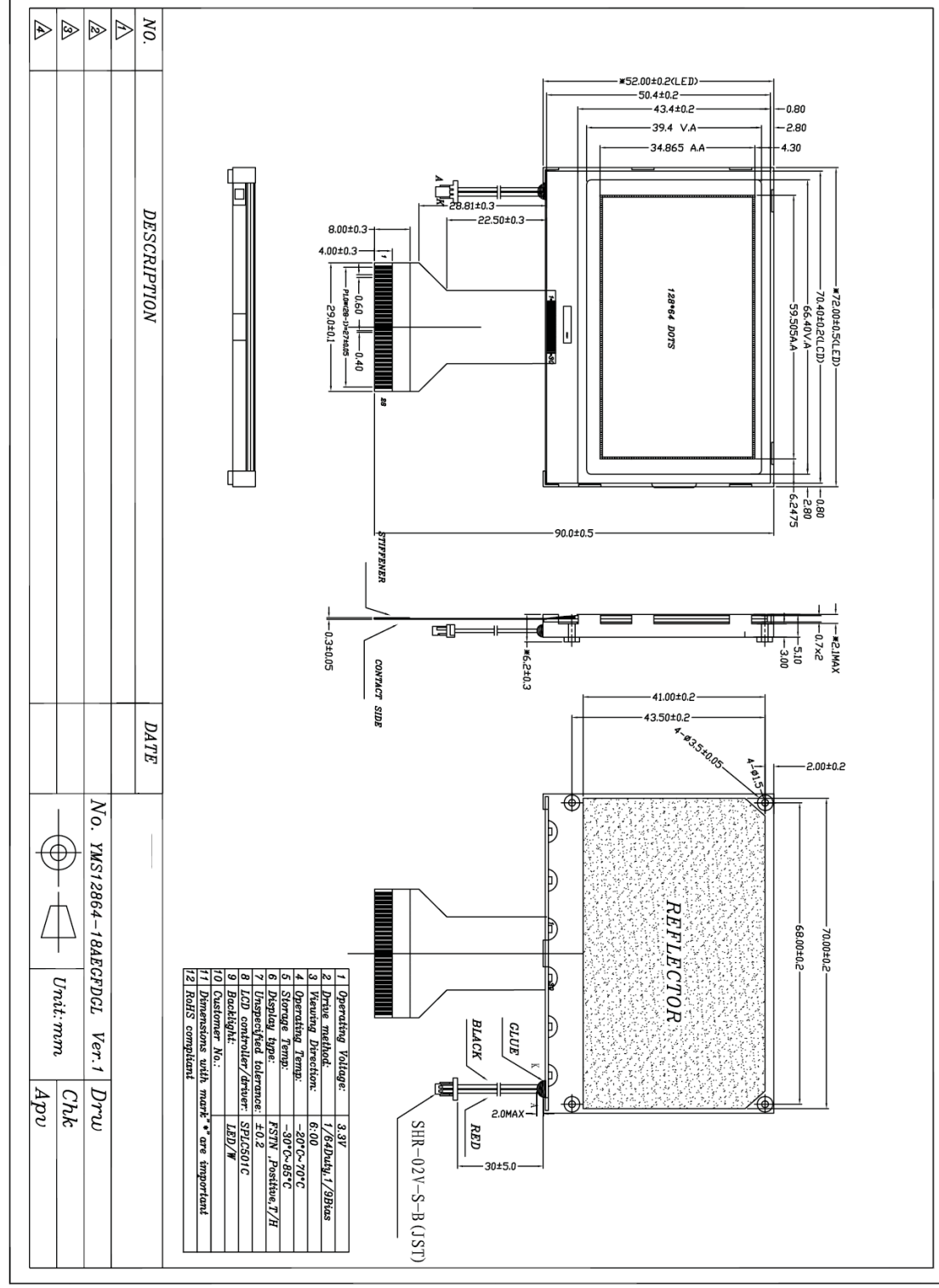
5	Pinhole		0.15＜Φ≤0.2 N≤1 0.05＜Φ≤0.15 N≤3 Φ≤0.05 Any number Note: Distance between two spots ≥10mm ，Φ〈1/3 pixels

7.Inspection Item

Item	The Standard Of Quality Inspection	Checking Method	Quantity Ratio
Frame	Smooth and even surface,no crack,no scratch,no rusty,and not be wrenched out of shape.the range between convex and concave is:d≤0.35mm,and the frame must be connected with the ground pad.	Checking With Eyes And Using Vernier Caliper, Multimeter	100%
The Relative Position of LCD and Frame	The end seal of the LCD must be at the same side with the frame's opening.	Checking With Eyes	100%
The Relative Position of PCB/Panel /Frame	The frame installing direction must be correct.the twisted angle of the leg is from 45° to 60° ,the leg is vertical to PCB panel and it must be in the middle position of the installing holes.	Checking With Eyes	100%
LED	1.The LED must be White 2.The LED must be uniform.	Checking With Eyes	100%
Function Test	1. The major defects must be reject. 2. Background changes evenly and no disorderly displaying phenomenon. 3. Display no shortage.	Check It When Displaying	100%

V .Attached Drawing

CUSTOMER'S APPROVED:	DATE:	PAGE:



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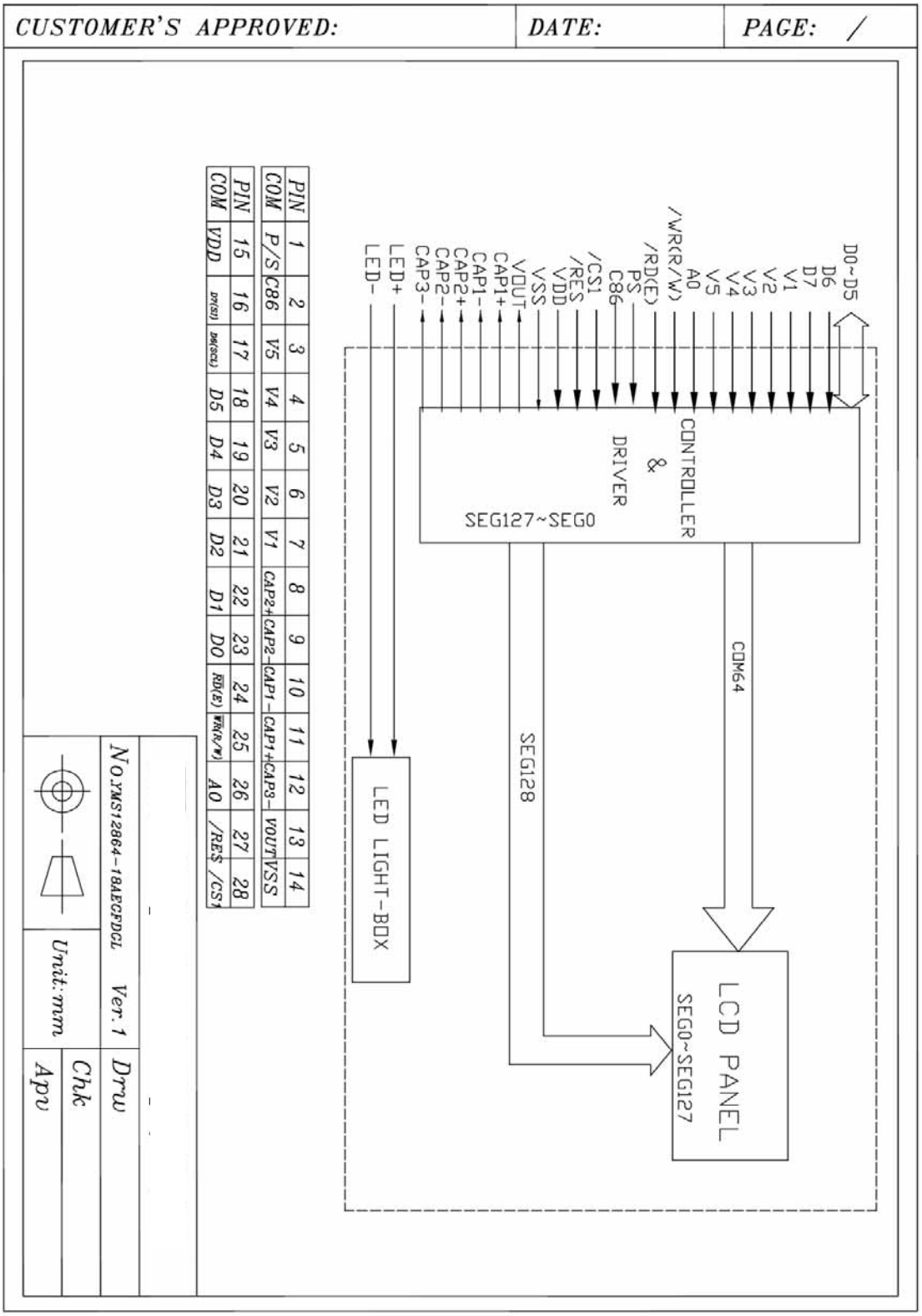


PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14
COM	P/S	C86	V5	V4	V3	V2	V1	CAP2+	CAP2-	CAP1-	CAP1+	CAP3-	VOUT	VSS

PIN	15	16	17	18	19	20	21	22	23	24	25	26	27	28
COM	VDD	SPI(SI)	IM0(SCL)	D5	D4	D3	D2	D1	D0	RD(E)	WR(R/W)	A0	/RES	/CS1

	No.YMS12864-18AEGFDGL	Ver.1
Unit:mm		Drw
		Chk
		Apv

Ⅵ.Packing

CUSTOMER'S APPROVED:	DATE: 2015.09.02	PAGE: 1/1

PRODUCT PART NO.:YMS12864-18AEGFDGL

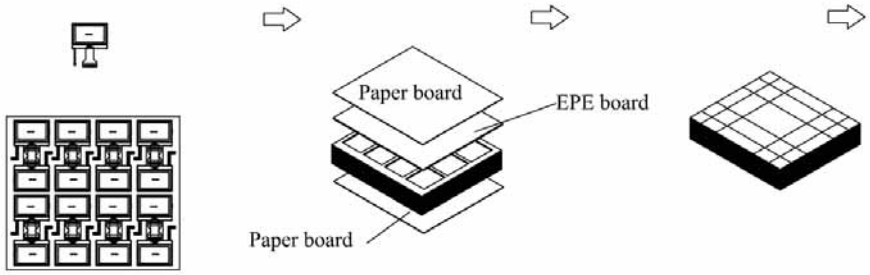
PACKING TYPE: BY EPE TRAY(T12864-18A)

PACKLING ORDER:

1) Putting 16 pcs Modules on each EPE tray.

2) Putting 7 pcs EPE trays together with EPE paper on the top of EPE tray.

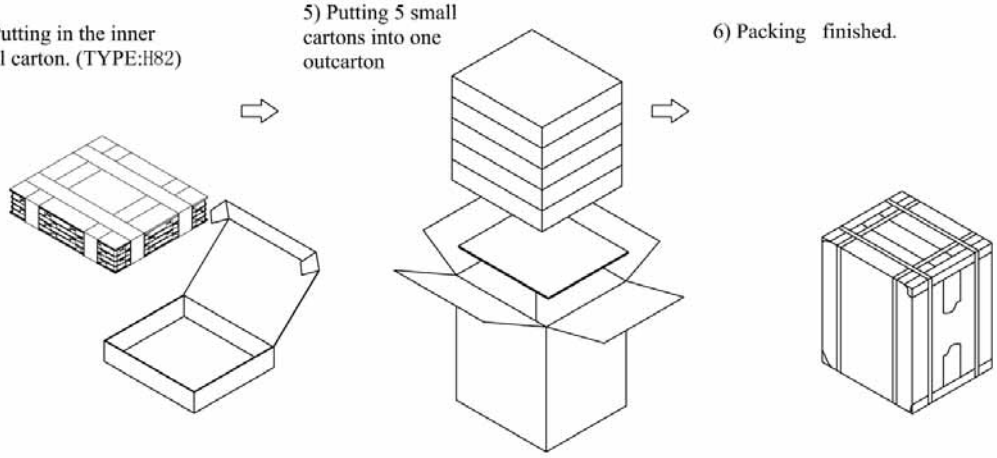
3) Assembling the boards and the tray together with adhesive tape



4) Putting in the inner small carton. (TYPE:H82)

5) Putting 5 small cartons into one outcarton

6) Packing finished.



Note: 16 pcs in a tray,7 trays in a inner carton,5 inner cartons in a out carton, so 16x7x5=560pcs/Outcarton

Dimension (Small carton): 385*325*87mm Dimension (Out carton): 394*344*470mm

NO. YMS12864-18AEGFDGL Ver.1	Drw:		Chk:		Apv:	

Ⅶ.Precautions For Use

1. Safety

(1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.

(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.

(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

2.Storage Conditions

(1) Store the panel or module in a dark place where the temperature is 25±5°C and the humidity is 50±20%RH.

(2) Store in anti-static electricity container.

(3) Store in clean environment, free from dust, active gas, and solvent.

(4) Do not place the module near organics solvents or corrosive gases.

(5) Do not crush, shake, or jolt the module.

(6) Do not exposed to direct sun light of fluorescent lamps.

3.Installing LCD Module

Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate or touch panel to protect the polarizer and LC cell.

(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements.

4.Precautions For Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (Vo). Adjust Vo to show the best contrast.

(2) Driving the LCD in the voltage above the limit will shorten its lifetime.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) When turning the power on, input each signal after the positive/negative voltage becomes stable.

(5) Do not apply water or any liquid on product which composed of T/P.

5.Handling Precautions

(1) Avoid static electricity which can damage the CMOS LSI; please wear the wrist strap when handling.

(2) The polarizing plate of the display is very fragile. so, please handle it very carefully.

(3) Do not give external shock.

(4) Do not apply excessive force on the surface; it may cause display abnormal .

(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

(7) Do not operate it above the absolute maximum rating.

(8) Do not remove the panel or frame from the module.

(9) Do not apply water or any liquid on product which composed of T/P.