



Mono FSTN Display Module

Product Specification

Part No. YMC-240128-78ABAFDGL

240 x 128 FSTN Display

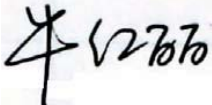

For more information, please visit www.andersdx.com
or email info@andersdx.com

Version 1.1

LIQUID CRYSTAL DISPLAY MODULE

MODEL NO.: YMC240128-78ABAFDGL

DATE: JAN.21.2014

Approved	Checked	Department
		

CUSTOMER:

MODEL NO.:

DATE:

Approved	Checked	Department

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 1 of 21

REVISION HISTORY

Rev.	Date	Item	Page	Remark
1.0	JAN.13.2014	New Creating	All	
1.1	JAN.21.2014	Spec didn't mentioned this item before	Not relate	Add aluminum foil to the backlight

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 2 of 21

LIST

I . General Specifications -----(3-7)

II . The Characteristics and Reliability Test -----(8-9)

III. The Equipment and LCD Measuring Method-----(10-11)

IV. Standard Specifications for Product Quality -----(12-15)

V .Attached Drawing -----(16-17)

VI.Packing----- (18)

- VII. Precautions For Use -----(19-20)

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 3 of 21

I .General Specifications

1. The Features :

- (1). The module operating voltage: 3.0V
- (2). Drive method: 1/128 duty, 1/12 bias
- (3). Viewing direction: 6:00
- (4). Operating temperature: 0°C~50°C
- (5). Storage temperature: -10°C~60°C
- (6). Display type: FSTN mode, Transflective, Positive type display

2. Mechanical Data:

- (1) Module Size ----- 98.00 (w) *67.00 (h) mm
- (2) Viewing Area ----- 92.00 (w) *53.00 (h) mm
- (3) Dot Size ----- 0.325 (w) * 0.325 (h) mm
- (4) Dot Quality----- 240* 128 DOTS
- (5) Outline Dimensions----- See Attached Drawing

3. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Logic Supply voltage	-0.3	+4.0	V
V _{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V _{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
V _{DD2/3} -V _{DD}	Voltage difference between V _{DD} and V _{DD2/3}	--	1.6	V
V _{LCD}	LCD Generated voltage (-30°C ~ +80°C)	-0.3	+17.0	V
V _{IN}	Any input voltage	-0.4	V _{DD} + 0.5	V

Note:

1. V_{DD} based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 4 of 21

4. Pin Connections:

Pin No.	Symbol	Function																																												
1	A	LED backlight																																												
2	K	LED backlight																																												
3	VB1-	LCD Bias Voltages																																												
4	VB1+	LCD Bias Voltages																																												
5	VB0-	LCD Bias Voltages																																												
6	VB0+	LCD Bias Voltages																																												
7	VLCD	Main LCD Power Supply.																																												
8	VBIAS	This is the reference voltage to generate the actual SEG driving voltage.																																												
9	VSS	Ground.																																												
10	VDD	Power supply																																												
11-18	D7-D0	Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,																																												
		<table border="1"> <thead> <tr> <th></th> <th>BM=1x (Parallel)</th> <th>BM=0x (Parallel)</th> <th>BM=01 (S9)</th> <th>BM=00 (S8/S8uc)</th> </tr> </thead> <tbody> <tr> <td>D0</td> <td>D0</td> <td>D0/D4</td> <td>SCK</td> <td>SCK</td> </tr> <tr> <td>D1</td> <td>D1</td> <td>D1/D5</td> <td>–</td> <td>–</td> </tr> <tr> <td>D2</td> <td>D2</td> <td>D2/D6</td> <td>–</td> <td>–</td> </tr> <tr> <td>D3</td> <td>D3</td> <td>D3/D7</td> <td>SDA</td> <td>SDA</td> </tr> <tr> <td>D4</td> <td>D4</td> <td>–</td> <td>–</td> <td>–</td> </tr> <tr> <td>D5</td> <td>D5</td> <td>–</td> <td>–</td> <td>–</td> </tr> <tr> <td>D6</td> <td>D6</td> <td>–</td> <td>S9</td> <td>S8/S8uc</td> </tr> <tr> <td>D7</td> <td>D7</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9)	BM=00 (S8/S8uc)	D0	D0	D0/D4	SCK	SCK	D1	D1	D1/D5	–	–	D2	D2	D2/D6	–	–	D3	D3	D3/D7	SDA	SDA	D4	D4	–	–	–	D5	D5	–	–	–	D6	D6	–	S9	S8/S8uc	D7	D7	0	1
	BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9)	BM=00 (S8/S8uc)																																										
D0	D0	D0/D4	SCK	SCK																																										
D1	D1	D1/D5	–	–																																										
D2	D2	D2/D6	–	–																																										
D3	D3	D3/D7	SDA	SDA																																										
D4	D4	–	–	–																																										
D5	D5	–	–	–																																										
D6	D6	–	S9	S8/S8uc																																										
D7	D7	0	1	1																																										
		Connect unused pins to V _{DD} or V _{SS} .																																												
19-20	WR1、WR0	WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail. In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V _{SS} .																																												
21	CD	Select Control data or Display data for read/write operation.																																												
22	RST	Reset signal																																												
23	CS	Chip select																																												

DATE JAN.21.2014

TECHNICAL
SPECIFICATION

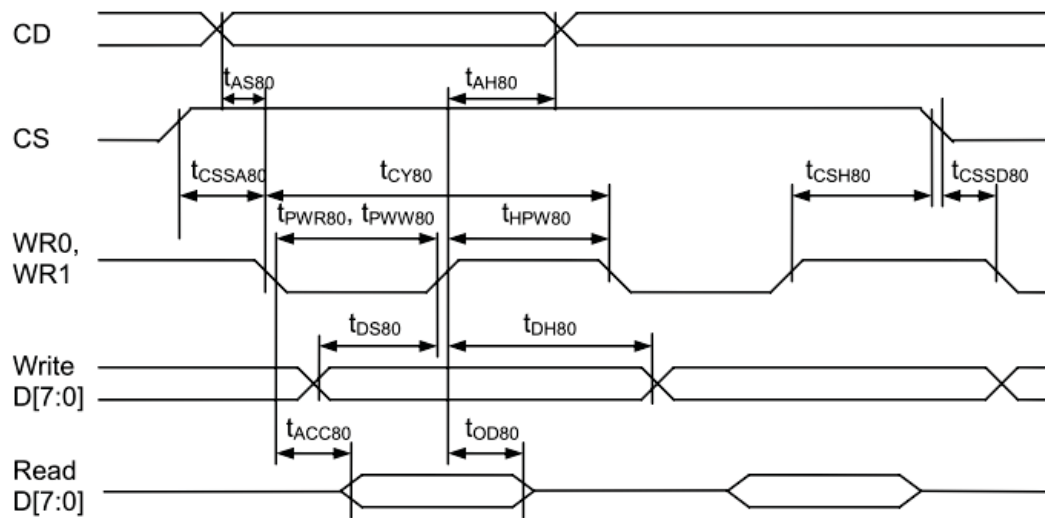
LCM

YMC240128-78ABAFDGL

Page 5 of 21

24-25	BM0、BM1	Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:		
		BM[1:0]	D[7:6]	Mode
		11	Data	6800/8-bit
		10	Data	8080/8-bit
		01	0X	6800/4-bit
		00	0X	8080/4-bit
		01	10	3-wire SPI w/ 9-bit token (S9: conventional)
		00	10	4-wire SPI w/ 8-bit token (S8: conventional)
00	11	3- or 4-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)		

5. AC CHARACTERISTICS

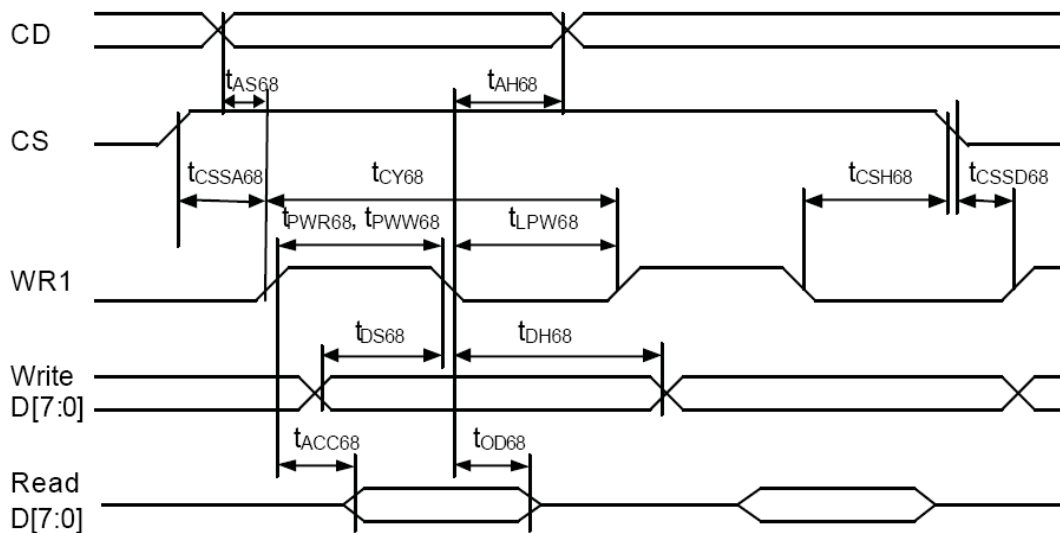


Parallel Bus Timing Characteristics (for 8080 MCU)

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 6 of 21

($2.7V \leq V_{DD} < 3.6V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80}	CD	Address setup time		0	-	nS
t_{AH80}		Address hold time		20	-	nS
t_{CY80}		System cycle time			-	nS
		8-bit bus (read)		140		
		8-bit bus (write)		140		
		4-bit bus (read)		140		
t_{PWR80}	WR1	Pulse width			-	nS
		8-bit bus (read)		65		
t_{PWW80}	WR0	Pulse width			-	nS
		4-bit bus (write)		35		
t_{HPW80}	WR0, WR1	High pulse width			-	nS
		8-bit bus (read)		65		
		(write)		35		
		4-bit bus (read)		65		
t_{DS80}	D0~D7	Data setup time		30	-	nS
		Data hold time		20	-	nS
t_{ACC80}		Read access time	$C_L = 100pF$	-	60	nS
t_{OD80}		Output disable time		12	20	nS
t_{SSA80}	CS1/CS0	Chip select setup time		10		nS
t_{CSSD80}				10		
t_{CSH80}				20		

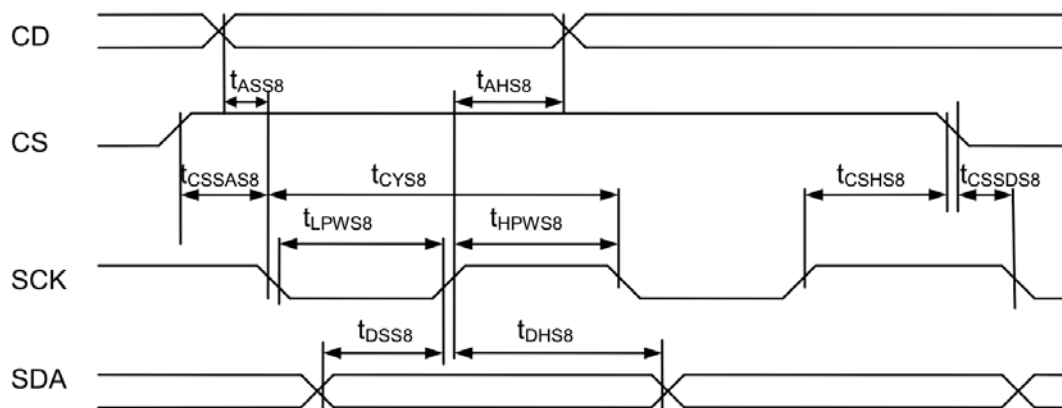


Parallel Bus Timing Characteristics (for 6800 MCU)

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 7 of 21

($2.7V \leq V_{DD} < 3.3V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68}	CD	Address setup time		0	–	nS
t_{AH68}		Address hold time		20	–	nS
T_{CY68}		System cycle time			–	nS
		8 bits bus (read)		140		
		(write)		140		
		4 bits bus (read)		140		
t_{PWR68}	WR1	Pulse width 8 bits (read)		65		
		4 bits		65	–	nS
t_{PWW68}		Pulse width 8 bits (write)		35	–	nS
		4 bits		35		
t_{LPW68}		Low pulse width			–	nS
		8 bits bus (read)		65		
		(write)		35		
		4 bits bus (read)		65		
t_{DS68}	D0~D7	Data setup time		30	–	nS
		t_{DH68}	Data hold time		20	
t_{ACC68}		Read access time	$C_L = 100pF$	–	60	nS
t_{OD68}		Output disable time		12	20	nS
t_{CSSA68}	CS1/CS0	Chip select setup time		10		nS
t_{CSSD68}				10		
t_{CSH68}				20		



Serial Bus Timing Characteristics (for S8 / S8uc)

($2.7V \leq V_{DD} < 3.6V$, $T_a = -30$ to $+85^\circ C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		20	–	nS
t_{CYS8}	SCK	System cycle time		140	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8}	SDA	Data setup time		30	–	nS
t_{DHS8}		Data hold time		20		
t_{CSSAS8}	CS	Chip select setup time		10		nS
t_{CSSDS8}				20		
t_{CSHS8}				10		

DATE JAN.21.2014

TECHNICAL SPECIFICATION

LCM

YMC240128-78ABAFDGL

Page 8 of 21

II .The Characteristics and Reliability Test

1. Electro-Optic Characteristics

Condition:TEMP=(23±3)°C

NO	Item	Symbol	Min.	Typ.	Max.	Unit	Condition
1	Supply Voltage(Logic)	Vdd-Vss		3.0		V	
2	LCD Operating Voltage	V ₀ -Vss		14.8		V	0°C
			14.4	14.6	14.8	V	25°C
				14.4		V	50°C
3	Response Time	Ton		150		ms	
		Toff		220		ms	
4	Contrast Ratio	CR	2	4			
5	Viewing Angle	12H	θ 1	30		Deg.	(CR≥2.0)
		6H	θ 2	40			
		3H	θ 3	40			
		9H	θ 4	30			

2.- Characteristics of backlight

Color: White

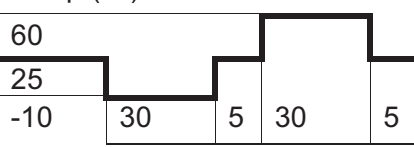
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	Vf	3.2	3.5	3.7	V	If=75mA
Power Dissipation	Pd	---	0.2625	0.2775	W	
Reverse Voltage	Vr	---	---	5.0	V	Vr=5.0V Each chip
Reverse Current	Ir	---	---	10	uA	
Luminous Intensity	Lv	250	330	450	cd/m ²	If=75mA
Luminous Uniformity	ΔLv	70	---	---	%	
Chromaticity coordinate	X	X=0.260	---	X=0.320		Each chip If=20mA Ta=25° C
	Y	Y=0.260	---	Y=0.320		

WARNING:

A BACKLIGHT IS A KIND OF CURRENT DEVICE,IT MUST CONNECT A RESISTANCE FOR LIMITING CURRENT ,OR IT WILL BE DAMAGED.

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 9 of 21

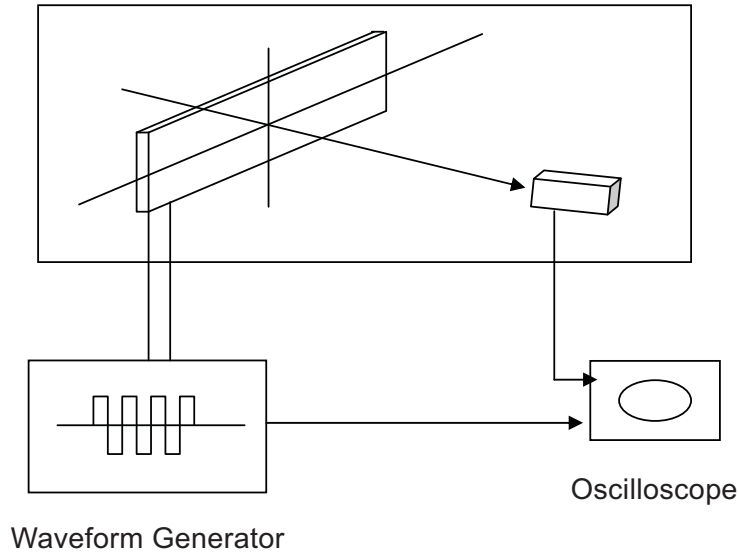
3. Reliability Test

No	Items	Test Condition	Test Result
1	High Temp Storage	Temp: $60 \pm 2^\circ\text{C}$ Time: 96h Restore: 24h	Passed
2	Low Temp Storage	Temp: $-10 \pm 3^\circ\text{C}$ Time: 96h Restore: 24h	Passed
3	High Temp operating	Temp: $50 \pm 2^\circ\text{C}$ Vop: 3.0V Time: 24h Restore: 24h	Passed
4	Low Temp operating	Temp: $0 \pm 3^\circ\text{C}$ Vop: 3.0V Time: 24h Restore: 24h	Passed
5	High Temp High Hum Storage	Temp: $40 \pm 2^\circ\text{C}$ Hum: 95%Rh Time: 96h Restore: 24h	Passed
6	Thermal Shock	Temp: ($^\circ\text{C}$)  5 Cycles Restore: 24h	Passed

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 10 of 21

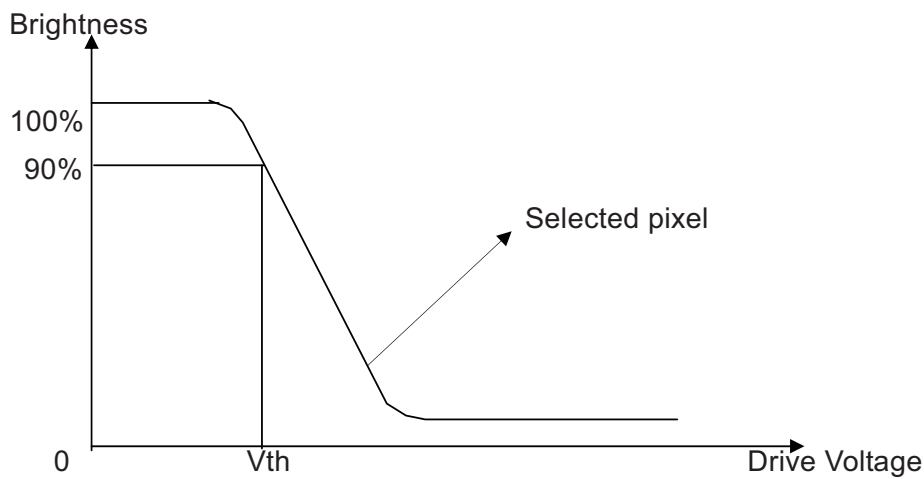
III. The Equipment and LCD Measuring Method

1. Equipment



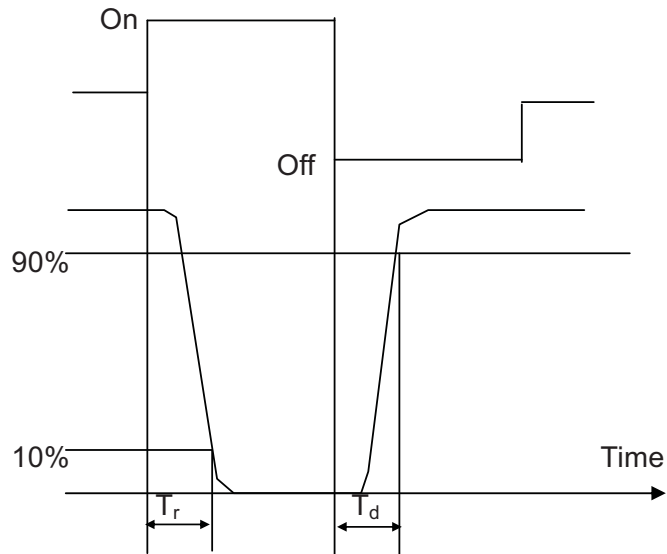
2. Definition

(1). Threshold Voltage (V_{th})

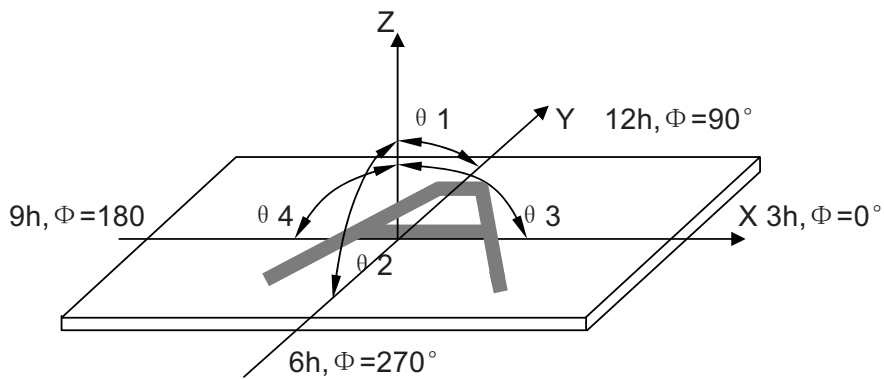


DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 11 of 21

(2). Response Time



(3). Viewing Angle:



(4). Contrast Ratio (Positive)

$$CR = \frac{\text{Brightness of non-selected pixel}}{\text{Brightness of selected pixel}}$$

3. Reliability Test:

Equipment : TENNY

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 12 of 21

IV. Standard Specifications for Product Quality

1. Manner of test:

- 1.1 The test must be under 40W fluorescent light, and the distance of view must be at 30cm.
- 1.2 The test direction is based on around -10°- 30° of Vertical line.

2. Quality specification

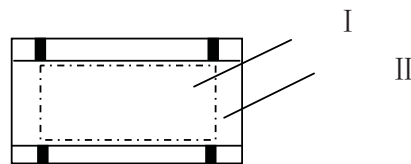
It shall be based on GB2828-87, Apply level II, Normal inspection by single sampling.

	IETM	CHECK LEVEL	AQL
MAJOR (MA)	1.LIQUID CRYSTAL LEAKAGE 2.WRONG POLARIZER 3.OUTSIDE DIMENSION 4.SEGMENT MISSING 5.SEGMENT SHORT	II	0.25
MINOR (MI)	1.BLACK SPOTS OR WHITE SPOTS. 2.FOREIGN SUBSTANCE, 3.WHITE SPOTS, 4.PINHOLE, SEGMENT 5.DEFORMATION SCRATCHS(GLASS & POLARIZER), 6.SEGMENT DEFECT, 7.AIR BUBBLES BETWEEN GLASS & POLARIZER, 8.COLOR VARIATION, GLASS CHIPS, 9.OTHER VISUAL DEFECTS.	II	1.0

3. Definition of area:

3.1 I area: viewing area

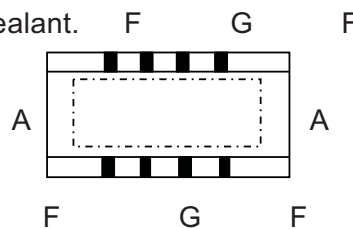
II area: outside viewing area



3.2 A area: The glass area outside sealant.

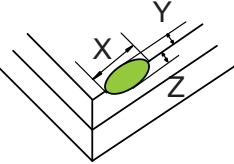
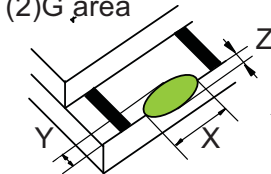
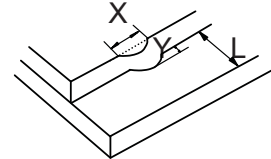
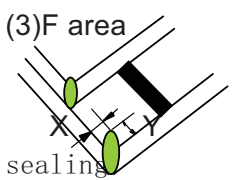
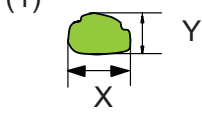
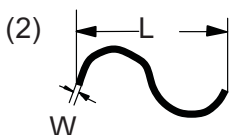
G area: Electrode pad area.

F area: Without electrode pad area.




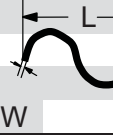
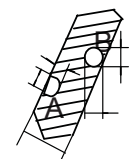
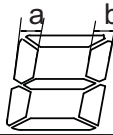
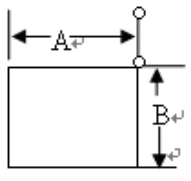
DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 13 of 21

4. Standard of appearance test: (unit: mm)

No	Items	Criterion	Checking manner
1	Substrate crack X: defect Length Y: defect Width Z: defect Depth T: glass Thickness N: defect QTY L: Connector Width	<p>(1) A area</p>  <p>$X \leq 3.0$ Y: Don't allowed hurt sealing $Z \geq T/2$ $N \leq 3$ $X \leq 5.0$ Y: Don't allowed hurt sealing $Z \leq T/2$ $N \leq 3$ $X \leq 1.0$ $Y \leq 0.5$ $Z \leq T/3$ No check</p> <p>(2) G area</p>  <p>$X \leq 3.0$ $Y \leq 0.5$ $Z \leq T/2$ $N \leq 2$</p>  <p>$X \leq \text{total length}$ $Y \leq 1/4L$ $N \leq 1$ Over the drawing tolerance is not allowed</p> <p>(3) F area</p>  <p>$X \leq 2.0$ $Y \leq 3$ $Z \leq T$ $N \leq 3$ Don't allowed hurt sealing</p>	checking with eyes
2	Black spot white spot $D = (X+Y)/2$ Line	<p>(1)</p>  <p>$0.2 < D \leq 0.25$ $N \leq 1$ $0.1 < D \leq 0.2$ $N \leq 3$ $D \leq 0.1$ No check</p> <p>(2)</p>  <p>$L \leq 2.0$ $W \leq 0.03$ $N \leq 2$ $L \leq 1.0$ $W \leq 0.05$ $N \leq 1$</p>	Checking on the table with light and polarizer and checking with eyes directly.
DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 14 of 21

No	Items	Criterion	Checking manner
3	Polarizer Bubble	$D \leq 0.15$ No check $0.15 < D \leq 0.4$ $N \leq 2$	Checking on the table with light and polarizer, and checking with eyes directly
4	Rainbow Color	Allow tiny rainbow Allow 5% color contrast or accord limitative sample	Checking on the table with light and polarizer, And checking with eyes directly
5	END Seal	1. Dimension accord design require 2. Inject depth (d): $1/5D \leq d \leq D$ (D: seal design depth)	Checking with eyes
6	Polarizer or pad appearance	No dirty	Checking with eyes

5 Standard of display test

No	Items	Criterion	Checking manner
1	Black spot white spot $D = (X+Y)/2$ Line	(1)  $0.2 < D \leq 0.25$ $N \leq 1$ $0.1 < D \leq 0.2$ $N \leq 3$ $D \leq 0.1$ No check (2)  $L \leq 2.0$ $W \leq 0.03$ $N \leq 2$ $L \leq 1.0$ $W \leq 0.05$ $N \leq 1$	Checking at the display state
2	Pin hole $D = (A+B)/2$ W: segment width	 $W \leq 0.4$ $D \leq 0.20$ And $D \leq 1/2W$ $N \leq 1$ $W > 0.4$ $D \leq 0.25$ And $D \leq 1/3W$ $N \leq 2$ $D \leq 0.05$ No check	Checking at the display state
3	Different width of segment	 $ a-b < 0.25$ or $ a-b \leq 1/4W$ No check	Checking at the display state
4	Different width		A: distortion $\leq 10\%$ B: distortion $\leq 10\%$ Superfluous Electrode lines display is not allowed

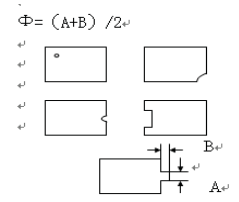
DATE JAN.21.2014

TECHNICAL SPECIFICATION

LCM

YMC240128-78ABAFDGL

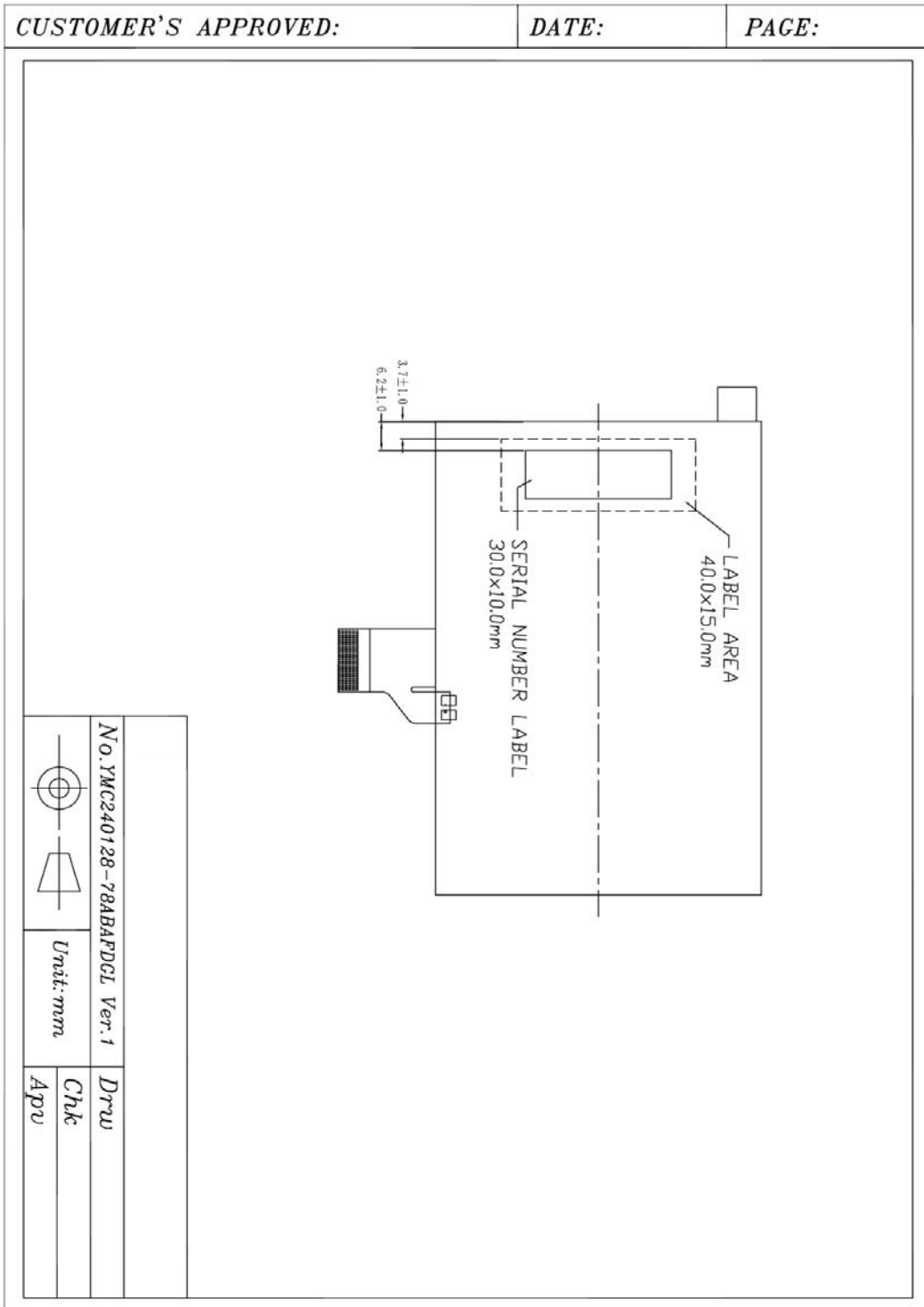
Page 15 of 21

5	Pinhole		$0.15 < \Phi \leq 0.2 \quad N \leq 1$ $0.05 < \Phi \leq 0.15 \quad N \leq 3$ $\Phi \leq 0.05$ Any number Note: Distance between two spots $\geq 10\text{mm}$, $\Phi < 1/3$ pixels
---	---------	---	---

6. Inspection Item and Standards

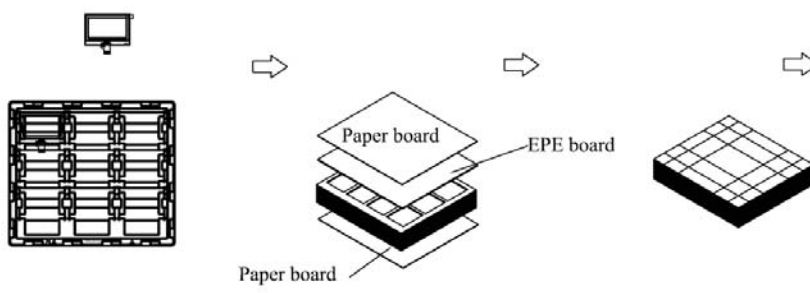
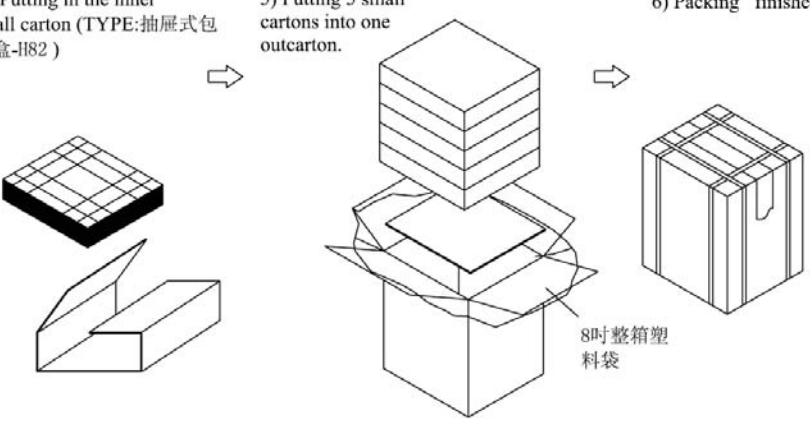
Item	The Standard Of Quality Inspection	Checking Method	Quantity Ratio
Frame	Smooth and even surface, no crack, no scratch, no rusty, and not be wrenched out of shape. The range between convex and concave is: $d \leq 0.35\text{mm}$, and the frame must be connected with the ground pad.	Checking With Eyes And Using Vernier Caliper, Multimeter	100%
The Relative Position of LCD and Frame	The end seal of the LCD must be at the same side with the frame's opening.	Checking With Eyes	100%
The Relative Position of PCB/Panel /Frame	The frame installing direction must be correct. The twisted angle of the leg is from 45° to 60° , the leg is vertical to PCB panel and it must be in the middle position of the installing holes.	Checking With Eyes	100%
LED	1. The LED must be White. 2. The LED must be uniform.	Checking With Eyes	100%
Function Test	1. The major defects must be reject. 2. Background changes evenly and no disorderly displaying phenomenon. 3. Display no shortage.	Check It When Displaying	100%

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 16 of 21



DATE JAN.21.2014		TECHNICAL SPECIFICATION
LCM	YMC240128-78ABAFDGL	Page 18 of 21

VI. Packing

<i>CUSTOMER'S APPROVED:</i>	<i>DATE: 2014.01.10</i>	<i>PAGE: 1/1</i>
<p>PRODUCT PART NO.: YMC240128-78ABAFDGL</p> <p>PACKING TYPE: BY PS TRAY(TPS240128-78A)</p> <p>PACKING ORDER:</p> <div style="display: flex; justify-content: space-around;"> <div style="width: 30%;"> <p>1) Putting 9 pcs Modules on each PS tray.</p> </div> <div style="width: 30%;"> <p>2) Putting 5 pcs EPE trays together with EPE paper on the top of EPE tray.</p> </div> <div style="width: 30%;"> <p>3) Assembling the boards and the trays together with adhesive tape.</p> </div> </div> <div style="text-align: center; margin: 10px 0;">  </div> <div style="display: flex; justify-content: space-around;"> <div style="width: 30%;"> <p>4) Putting in the inner small carton (TYPE:抽展式包装盒-1182)</p> </div> <div style="width: 30%;"> <p>5) Putting 5 small cartons into one outcarton.</p> </div> <div style="width: 30%;"> <p>6) Packing finished.</p> </div> </div> <div style="text-align: center; margin: 10px 0;">  </div> <p>Note: 9 pcs in a tray, 5trays in a inner carton, 5 inner cartons in a out carton, so 9x9x5=225pcs/Outcarton</p> <p>Dimension (Small carton): 360*320*82mm Dimension (Out carton): 394*344*470mm</p>		
NO. YMC240128-78ABAFDGL	Drw:	Chk:
		Apv:

DATE JAN.21.2014

TECHNICAL SPECIFICATION

LCM

YMC240128-78ABAFDGL

Page 19 of 21

VII. Precautions For Use

1. Safety

- (1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
- (2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
- (3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

2. Storage Conditions

- (1) Store the panel or module in a dark place where the temperature is $23\pm 5^{\circ}\text{C}$ and the humidity is below $50\pm 20\% \text{RH}$.
- (2) Store in anti-static electricity container.
- (3) Store in clean environment, free from dust, active gas, and solvent.
- (4) Do not place the module near organics solvents or corrosive gases.
- (5) Do not crush, shake, or jolt the module.
- (6) Do not exposed to direct sun light of fluorescent lamps.

3. Installing LCD Module

Attend to the following items when installing the LCM.

- (1) Cover the surface with a transparent protective plate or touch panel to protect the polarizer and LC cell.
- (2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements.

4. Precautions For Operation

- (1) Viewing angle varies with the change of liquid crystal driving voltage (V_0). Adjust V_0 to show the best contrast.
- (2) Driving the LCD in the voltage above the limit will shorten its lifetime.
- (3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
- (4) When turning the power on, input each signal after the positive/negative voltage

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 20 of 21

becomes stable.

(5) Do not apply water or any liquid on product which composed of T/P.

5.Handling Precautions

(1) Avoid static electricity which can damage the CMOS LSI; please wear the wrist strap when handling.

(2) The polarizing plate of the display is very fragile. so, please handle it very carefully.

(3) Do not give external shock.

(4) Do not apply excessive force on the surface; it may cause display abnormal .

(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

(7) Do not operate it above the absolute maximum rating.

(8) Do not remove the panel or frame from the module.

(9) Do not apply water or any liquid on product which composed of T/P.

DATE JAN.21.2014			TECHNICAL SPECIFICATION
LCM		YMC240128-78ABAFDGL	Page 21 of 21