Specification for Mono OLED Display module

2.80" Orange OLED Display module

Manufacturer	Truly Semiconductors LTD
Part n°	OEL9M1020-O-E
Ordering n°	OEL9M1020-O-E
Customer Part n°	n/a
Revision n°	1.0
Issue Date	2017/06/20

Customer's Approval

Company name	
Printed name	
Job title	
Signature	
Approval Stage:	This product is approved for the following production stage: - ☐ Sample / Prototype ☐ Pre-Production ☐ Mass Production
Approval Date	

Supplied by Anders Electronics plc
Manufactured by Truly Semiconductors LTD

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SPECIFICATION

PART NO. : OEL9M1020-O-E

OLED
Display
256 x 64
2.80"

This specification may be changed without any notice in order to improve performance or quality etc.
Please contact OLED R&D department TRULY Semiconductors LTD. For updated specification and product status before design for this product or release the order.

PRODUCT CONTENTS

TRULY®信利		Customer	
Written by	ChenYongquan	Approved by	
Checked by	Yang Xueyu		
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REVISION HISTORY

Rev.	Contents	Date
0.1	Preliminary Version	2016-12-15
1.0	First release.	2017-06-20

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	2.80	Inch
2	Resolution	256(H) x 64(V)	Dots
3	Active Area	17.26 (W) x 69.10(H)	mm^2
4	Outline Dimension (Panel)	28.50 (W) x 80.50(H)	mm^2
5	Pixel Pitch	0.270 (W) x 0.270(H)	mm^2
6	Pixel Size	0.245(W) x 0.245(H)	mm^2
7	Driver IC	SSD1362Z	-
8	Display Color	Orange	-
9	Gray scale	4	Bit
10	Interface	Parallel / Serial / IIC	-
11	IC package type	COG	-
12	Thickness	2.00±0.1	mm
13	Weight	TBD	g
14	Duty	1/64	-

■ ABSOLUTE MAXIMUM RATINGS

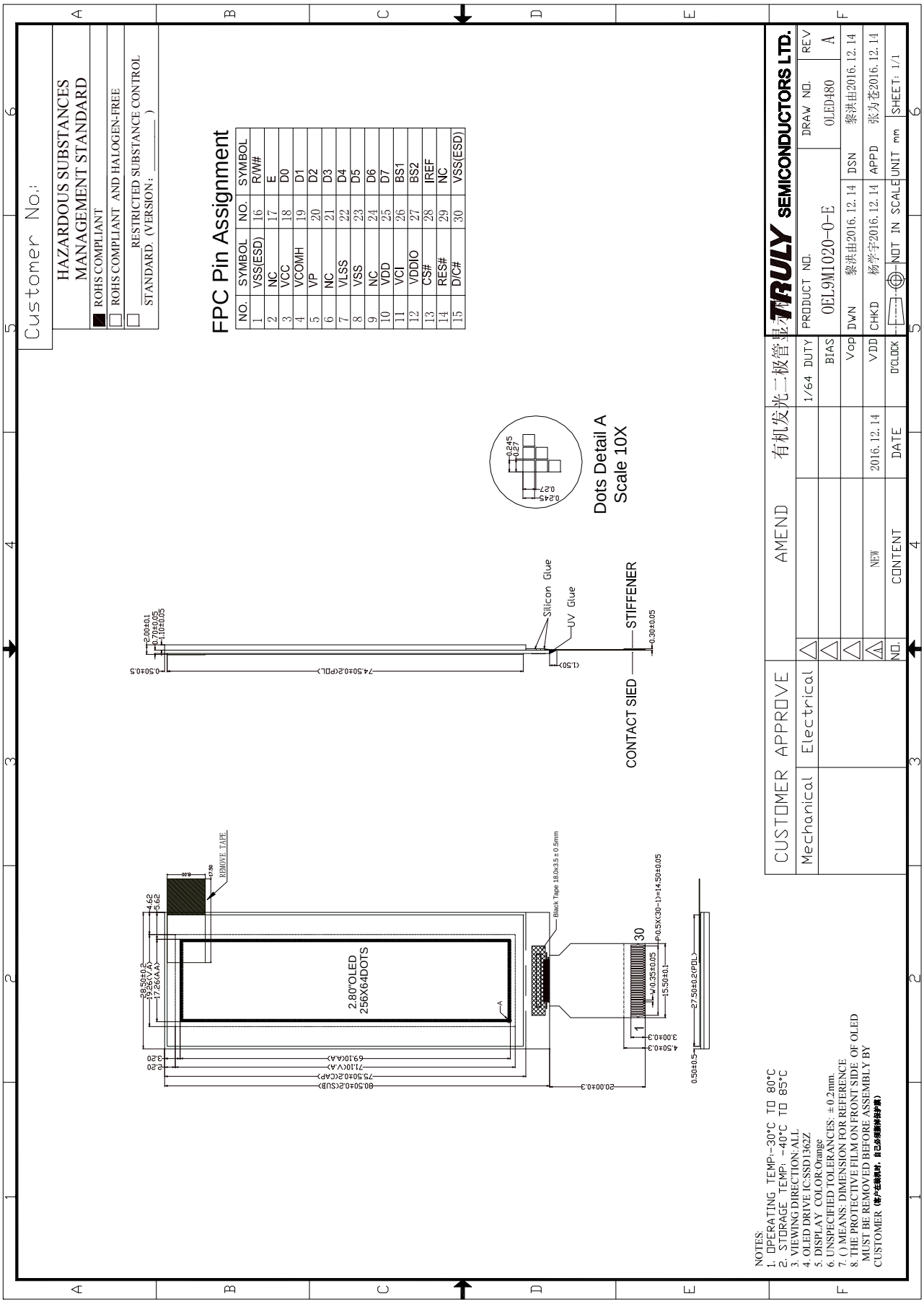
Unless otherwise specified, V_{SS} = 0V (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	VDD	-0.5	-	2.75	V
		VCI	-0.3	-	5.5	
	Driving	VCC	-0.5	-	21.0	V
Operating Temperature		Top	-30	-	80	℃
Storage Temperature		Tst	-40	-	85	℃
Humidity		-	-	-	90	%RH

Note:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Unless otherwise specified, V_{SS} = 0V, VCI=1.65V to 3.5V. (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	VDD	1.65	-	2.6	V
	Low Power	VCI	1.65	-	3.5	
	I/O Power	VDDIO	1.65	-	VCI	
	Driving	VCC	10.0	-	20.0	V
Input Voltage	High Voltage	V_{IH}	0.8 x VDDIO	-	-	V
	Low Voltage	V_{IL}	-	-	0.2 x VDDIO	V
Output Voltage	High Voltage	V_{OH}	0.9x VDDIO	-	-	V
	Low Voltage	V_{OL}	-	-	0.1 x VDDIO	V

◆AC Characteristics

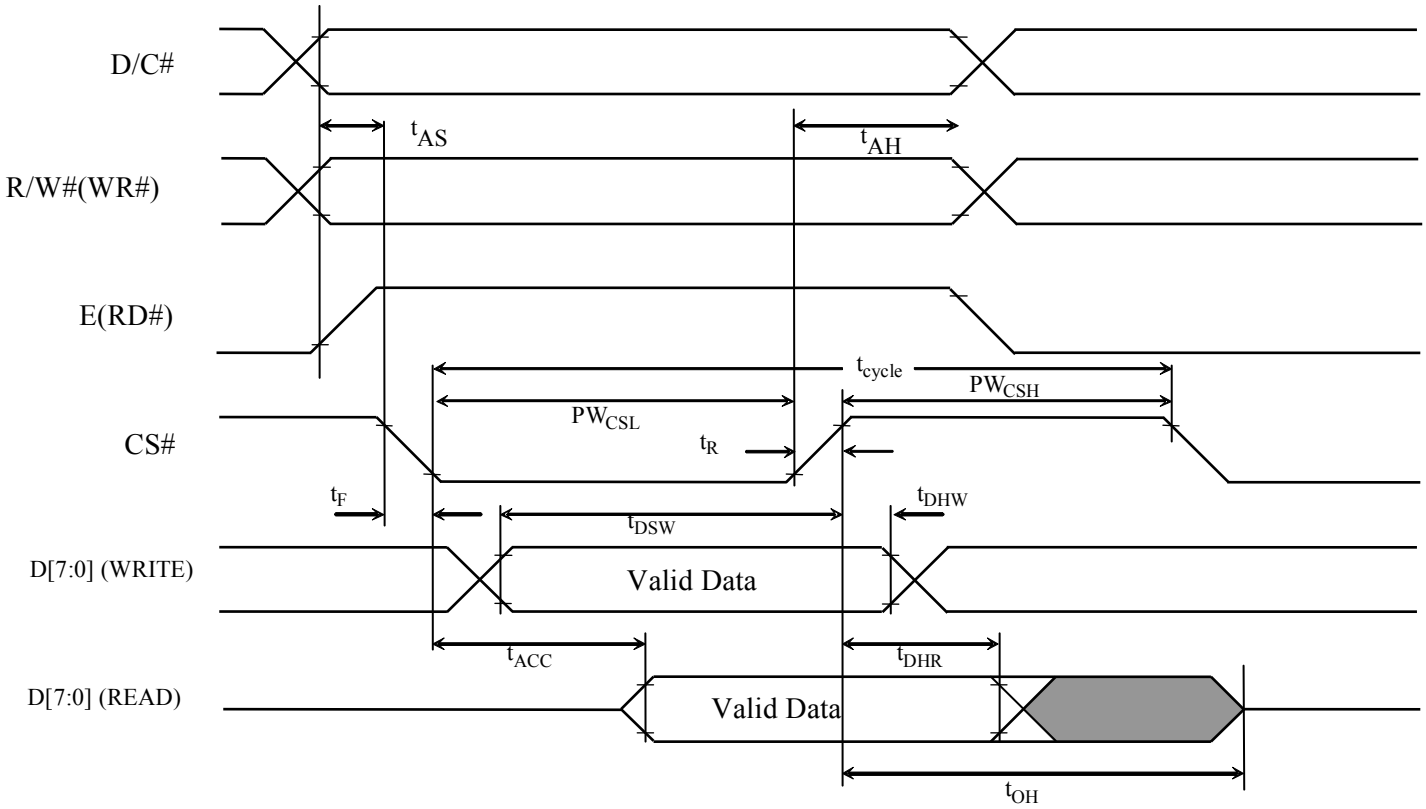
1. 6800-Series MCU Parallel Interface Timing Characteristics

6800-Series MCU Parallel Interface Timing Characteristics

V_{CI} - V_{SS} = 1.65V to 3.5V (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	320	-	-	ns
t_{AS}	Address Setup Time	25	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	45	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	250	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	160 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

6800-series MCU parallel interface characteristics



2. 8080-Series MCU Parallel Interface Timing Characteristics

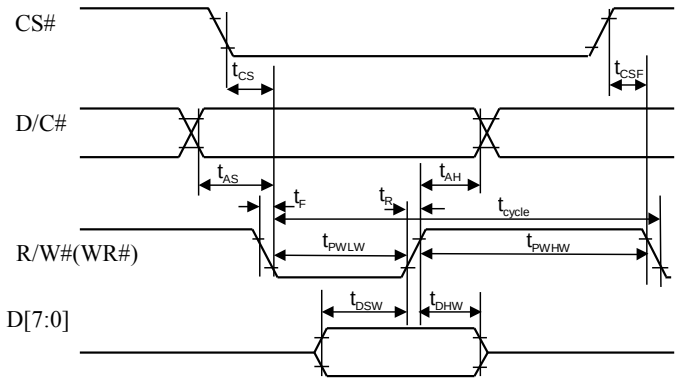
8080-Series MCU Parallel Interface Timing Characteristics

V_{CI} - V_{SS} = 1.65V to 3.5V (T_A = 25°C)

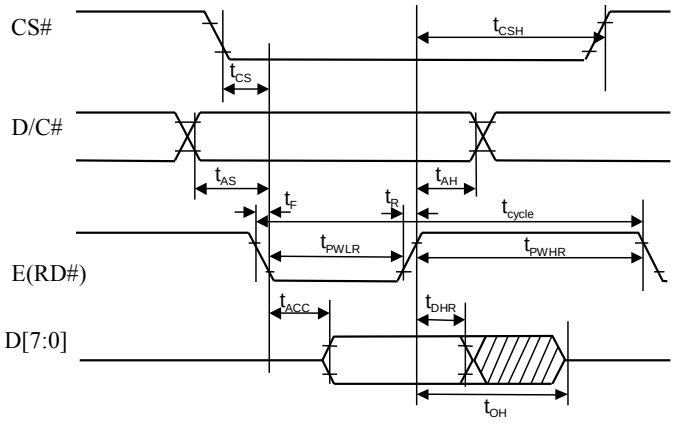
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle



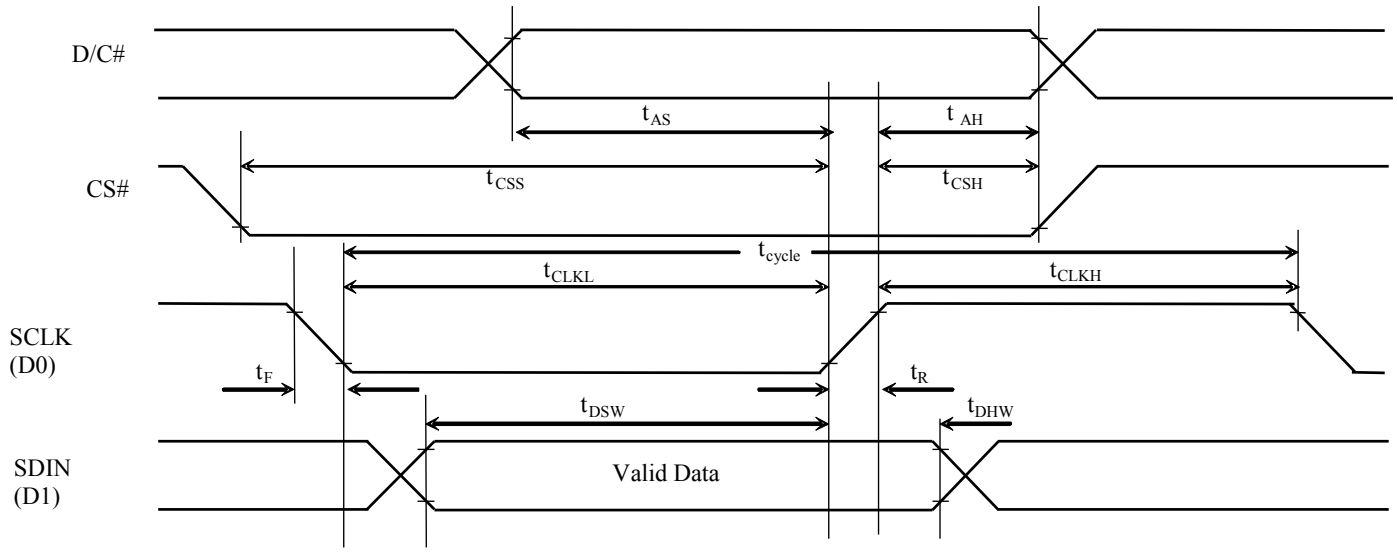
3. Serial Interface Timing Characteristics

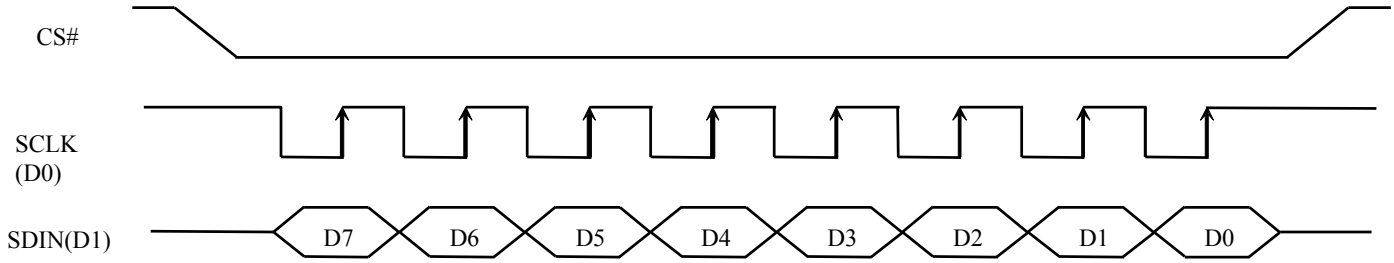
Serial Interface Timing Characteristics (4-wire SPI)

V_{CI} - V_{SS} = 1.65V to 3.5V (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	40	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (4-wire SPI)



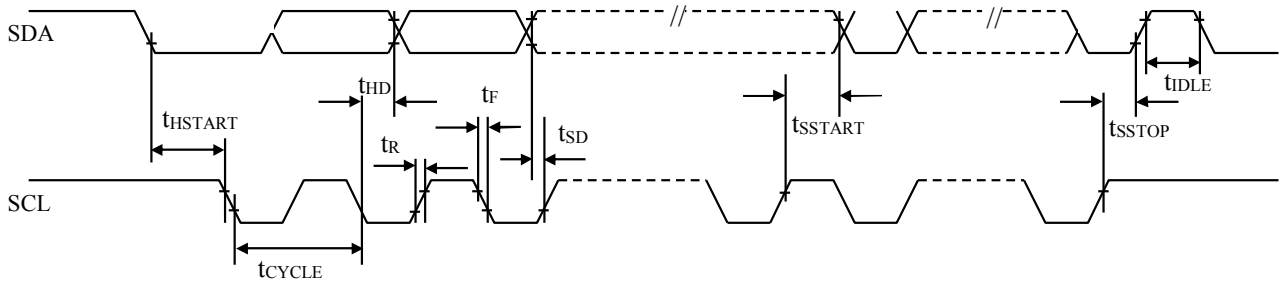


4. I²C Timing Characteristics

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I2C interface Timing characteristics



■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	80	100*	-	cd /m2	100% pixels ON
Power Consumption		P	-	250	350	mW	30% pixels ON L=100cd/m^2
Frame Frequency		Fr	-	100	-	Hz	-
Color Coordinate	Orange	CIE x	0.50	0.54	0.58	CIE1931	Color Coordinate
		CIE y	0.40	0.44	0.48		
Response Time	Rise	Tr	-	-	0.02	ms	Response Time
	Decay	Td	-	-	0.02	ms	
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	4,000	-	-	Hours	L=100cd/m2

Note:

1. L=100 cd/m^2 is based on V_{DD}=3.0V, Vcc=12.0V, contrast command setting 0xDF;

2. Contrast ratio is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. Life Time is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed).
(The initial value should be closed to the typical value after adjusting.)

■ INTERFACE PIN CONNECTIONS

No.	Symbol	Description
1	VSS (ESD)	Ground pin used for ESD. It must be connected to external ground.
2	NC	No connection.
3	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
4	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS. No external power supply is allowed to connect to this pin.
5	VP	This pin is the segment pre-charge voltage reference pin. A capacitor should be connected between this pin and VSS. No external power supply is allowed to connect to this pin.
6	NC	No connection.
7	VLSS	Analog system ground pin. It must be connected to external ground.
8	VSS	Ground pin. It must be connected to external ground.
9	NC	No connection.
10	VDD	Power supply for core logic operation. VDD can be supplied externally (within the range of 1.65V to 2.6V) or regulated internally from VCI when VCI is >2.6V. A capacitor should be connected between VDD and VSS under all circumstances.
11	VCI	Low voltage power supply. VCI must always be equal to or higher than VDD and VDDIO.
12	VDDIO	Power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source.
13	CS#	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW). In I2C mode, this pin must be connected to VSS.
14	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
15	D/C#	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D [7:0] will be interpreted as data. When the pin is pulled LOW, the data at D [7:0] will be transferred to a command register. In I2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to VSS.

16	R/W#	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
17	E	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
18	D0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID. When I2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
19	D1	
20	D2	
21	D3	
22	D4	
23	D5	
24	D6	
25	D7	
26	BS1	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2 and BS1 are pin select.
27	BS2	
28	IREF	This pin is the segment output current reference pin. When external IREF is used, a resistor should be connected between this pin and VSS to maintain current of around 18.75uA. When internal IREF is used, this pin should be kept NC.
29	NC	No connection.
30	VSS (ESD)	Ground pin used for ESD. It must be connected to external ground.

■ COMMAND TABLE

(R/W# (WR#) = 0, E(RD#) = 1 unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup Column start and end address A[6:0]: Start Address, range:00h~7Fh, (RESET = 00h) B[6:0]: End Address, range:00h~7Fh, (RESET = 7Fh)
0 0 0	75 A[5:0] B[5:0]	0 * *	1 * *	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Setup Row start and end address A[5:0]: Start Address, range:00h~3Fh, (RESET = 00h) B[5:0]: End Address, range:00h~3Fh, (RESET = 3Fh)
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
00 0	A0 A[7:0]	1 A_7	0 A_6	1 0	0 A_4	0 0	0 A_2	0 A_1	0 A_0	Set Re-map	Re-map setting in Graphic Display Data RAM (GDDRAM) A[0] = 0b, Disable Column Address Re-map (RESET) A[0] = 1b, Enable Column Address Re-map A[1] = 0b, Disable Nibble Re-map (RESET) A[1] = 1b, Enable Nibble Re-map A[2] = 0b, Enable Horizontal Address Increment (RESET) A[2] = 1b, Enable Vertical Address Increment A[4] = 0b, Disable COM Re-map (RESET) A[4] = 1b, Enable COM Re-map A[6] = 0b, Disable SEG Split Odd Even A[6] = 1b, Enable SEG Split Odd Even (RESET) A[7] = 0b, Disable SEG left/right remap (RESET) A[7] = 1b, Enable SEG left/right remap
0 0	A1 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	A[5:0]: Vertical shift by setting the starting address of display RAM from 0 ~ 63 (RESET = 00h)

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	A2 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	A[5:0]: Set vertical offset by COM from 0 ~ 63 (RESET = 00h) e.g. Set A[5:0] to 010000b to move COM16 towards COM0 direction for 16 row
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0]: Number of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). (RESET = 00h) B[6:0]: Number of rows in the scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. (RESET = 40h) Note (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3) Set Display Start Line (A[5:0] in A1h) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[5:0]=64 : whole area scrolls A[5:0]= 0, B[5:0] < 64 : top area scrolls A[5:0] + B[5:0] < 64 : central area scrolls A[5:0] + B[5:0] = 64 : bottom area scrolls
0	A4 ~ A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h = Normal display (RESET) A5h = All ON (All pixels have gray scale of 15, GS15) A6h = All OFF (All pixels have gray scale of 0, GS0) A7h = Inverse Display (GS0 fi GS15, GS1 fi GS14, GS2 fi GS13, …)
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set MUX Ratio	A[5:0]: Set MUX ratio from 4MUX ~ 64MUX: A[5:0] = 3 represents 4MUX A[5:0] = 4 represents 5MUX : A[5:0] = 62 represents 63MUX A[5:0] = 63 represents 64MUX (RESET) It should be noted that A[5:0]=0~2 is not allowed
0 0	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection A	A[0]=0b, Select external V_{DD} (i.e. Disable internal V_{DD} regulator) A[0]=1b, Enable internal V_{DD} regulator (RESET)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	AD A[4]	1 1	0 0	1 0	0 A_4	1 1	1 1	0 1	1 0	External / Internal I_{REF} Selection	Select external or internal I_{REF} : A[4] = '0' Select external I_{REF} (RESET) A[4] = '1' Enable internal I_{REF} during display ON
0	AE / AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh = Display OFF (sleep mode) (RESET) AFh = Display ON in normal mode
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0]: Phase 1 period of 2~30 DCLK's (i.e. 2, 4, 6, 8…30) (RESET = 0010b) A[7:4]: Phase 2 period of 2~30 DCLK's (i.e. 2, 4, 6, 8…30) (RESET = 1000b) **Note** (1) GS15 level pulse width must be set larger than the period of phase 1 + phase 2
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Front Clock Divider /Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) (i.e. 1, 2, 4, 8…256) (RESET is 0001b, i.e. divide ratio = 2) A[7:4]: Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (Range:0000b~1111b) (RESET = 1010b)
0 0	B5 A[3:0]	1 0	0 0	1 0	1 0	0 A_3	1 A_2	0 A_1	1 A_0	GPIO	A[1:0] = 00b represents GPIO0 pin HiZ, input disable (always read as low) A[1:0] = 01b represents GPIO0 pin HiZ, input enable A[1:0] = 10b represents GPIO0 pin output Low (RESET) A[1:0] = 11b represents GPIO0 pin output High A[3:2] = 00b represents GPIO1 pin HiZ, input disable (always read as low) A[3:2] = 01b represents GPIO1 pin HiZ, input enable A[3:2] = 10b represents GPIO1 pin output Low (RESET) A[3:2] = 11b represents GPIO1 pin output High
0 0	B6 A[3:0]	1 *	0 *	1 *	1 *	0 A_3	1 A_2	1 A_1	0 A_0	Set Second pre-charge Period	A[3:0]: Second Pre-charge period of 1~15 DCLK's e.g. A[3:0] = 1111b, 15 DCLK Clock (RESET = 0100b)

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 15 data bytes set the gray scale pulse width in unit of DCLK's. A1[7:0], value for GS1 level Pulse width A2[7:0], value for GS2 level Pulse width … A14[7:0], value for GS14 level Pulse width A15[7:0], value for GS15 level Pulse width **Note** (1) The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15 (2) GS15 level pulse width must be set larger than the period of phase 1 + phase 2 (3) GS15 level must be set larger than 140 (ie. 8Ch)
0	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
0	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
…	…	…	…	…	…	…	…	…	…		
…	…	…	…	…	…	…	…	…	…		
…	…	…	…	…	…	…	…	…	…		
0	A14[7:0]	$A14_7$	$A14_6$	$A14_5$	$A14_4$	$A14_3$	$A14_2$	$A14_1$	$A14_0$		
0	A15[7:0]	$A15_7$	$A15_6$	$A15_5$	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		
0	B9	1	0	1	1	1	0	0	1	Linear LUT	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 12; GS2 level pulse width =24; GS3 level pulse width = 36; : GS14 level pulse width = 168; GS15 level pulse width = 180
0	BC	1	0	1	1	1	1	0	0	Set Pre-charge voltage	Set pre-charge voltage level.
0	A[4:0]	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	BD	1	0	1	1	1	1	0	0	Pre-charge voltage capacitor Selection	A[0]=0b, Without external V_P capacitor (RESET) A[0]=1b, With external V_P capacitor
0	A[0]	0	0	0	0	0	0	0	A_0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	Set COM deselect voltage level.
0	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		

A[4:0]	Hex code	Pre-charge voltage
00000	00h	0.10 x V_{CC}
:	:	:
00100	04h	0.15 x V_{CC} (RESET)
:	:	:
11111	1Fh	0.51 x V_{CC}

A[3:0]	Hex code	V_{COMH}
0000	00h	0.72 x V_{CC}
:	:	:
0101	05h	0.82 x V_{CC} (RESET)
:	:	:
0111	07h	0.86 x V_{CC}

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command
0 0	23 A[5:0]	0 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Fade In / Out and Blinking	A[5:4] = 00b, Disable fade mode (RESET) A[5:4] = 01b, Enable fade in mode, Once Fade In Mode is enabled, enter a new contrast setting by 81h command and contrast will increase gradually to the target contrast setting. Output follows the latest contrast setting when Fade mode is disabled. Note: (1) The new contrast setting must be larger than the original contrast setting before Fade In Mode is enabled. A[5:4] = 10b, Enable fade out mode, Once Fade Out Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and then contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled. A[3:0], Set the time interval for each fade step A[3:0] / Time interval / step 0000 / 8 frames 0001 / 16 frames 0010 / 24 frames … / … 1110 / 120 frames 1111 / 128 frames

Note

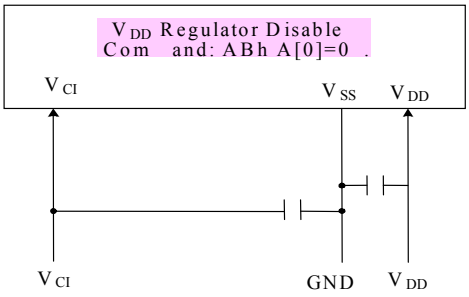
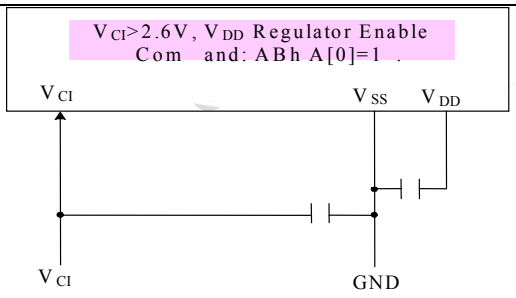
(1) "*" stands for "Don't care".

(2) VDD Regulator

In SSD1362, the power supply pin for core logic operation, VDD, can be supplied by external source or internally regulated through the VDD regulator.

The internal VDD regulator is enabled by setting bit A[0] to 1b in command ABh "Function Selection". VCI should be larger than 2.6V when using the internal VDD regulator. It should be noticed that, no matter VDD is supplied by external source or internally regulated; VCI must always be set equivalent to or higher than VDD.

The following table summarizes the input / output connection of VCI, VDDIO and VDD.

Pin Name	$V_{CI} \leq 2.6V$ Application	$V_{CI} > 2.6$ V Application
V_{CI}	1.65V – 2.6V	2.6V – 3.5V
V_{DD_IO}	1.65 V – V_{CI}	1.65V – V_{CI}
V_{DD}	1.65 V – V_{CI}	NC with stabilizing capacitor It is internally regulated
Pin connection scheme		

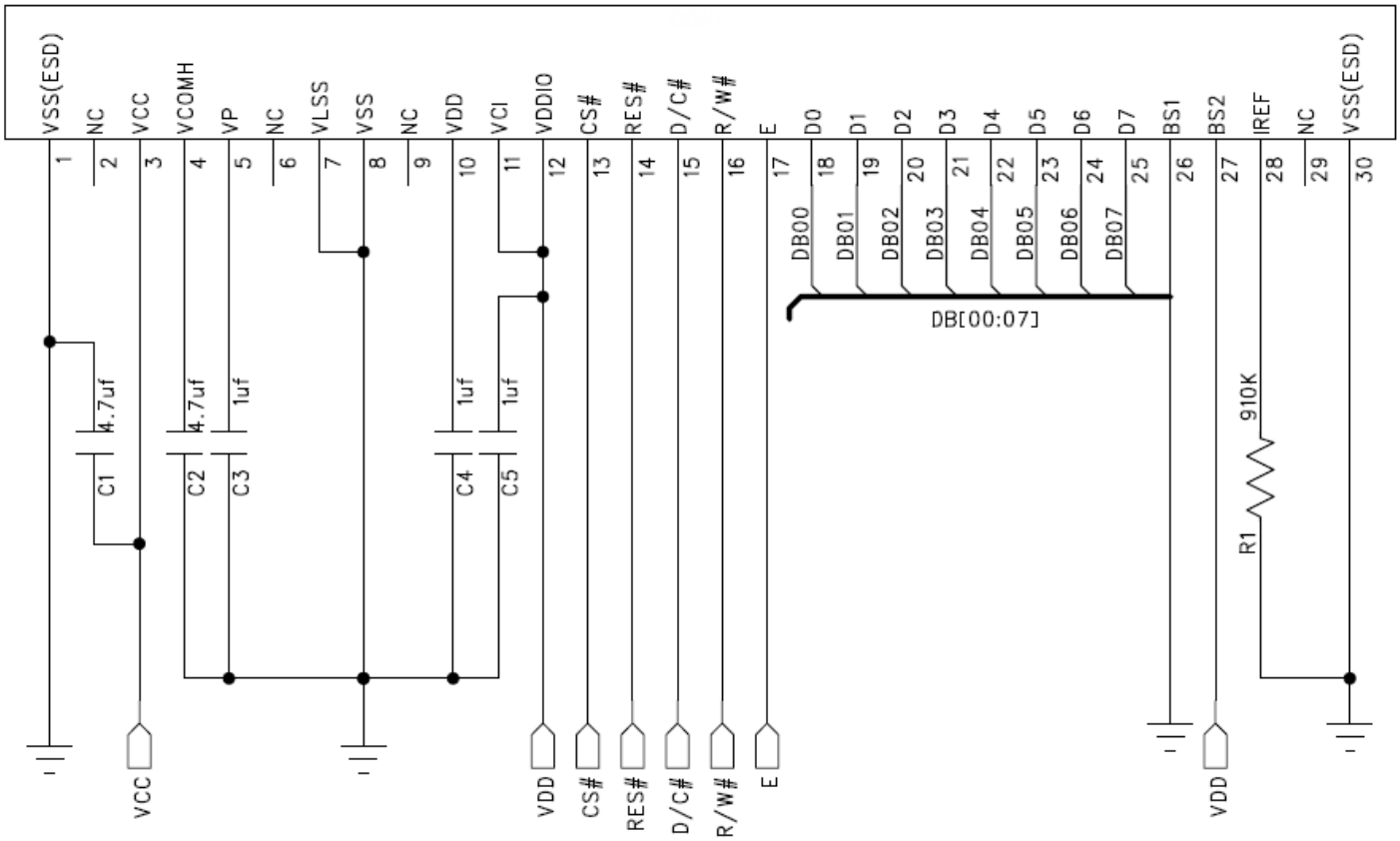
■ INITIALIZATION CODE

```
void Init_SSD1362(void)
{
    Write_Command(0XFD);            //Set Command Lock
    Write_Command(0X12);            //(12H=Unlock,16H=Lock)

    Write_Command(0XAE);            //Display OFF(Sleep Mode)

    Write_Command(0X15);            //Set Column Address
    Write_Command(0X00);          //Start Column Address
    Write_Command(0X7F);          //End Column Address

    Write_Command(0X75);            //Set Row Address
    Write_Command(0X00);          //Start Row Address
    Write_Command(0X3F);          //End Row Address

    Write_Command(0X81);            //Set Contrast
    Write_Command(CONTRAST);

    Write_Command(0XA0);            //Set Remap
    Write_Command(0XC1);

    Write_Command(0XA1);            //Set Display Start Line
    Write_Command(0X00);

    Write_Command(0XA2);            //Set Display Offset
    Write_Command(0X00);

    Write_Command(0XA4);            //Normal Display

    Write_Command(0XA8);            //Set Multiplex Ratio
    Write_Command(0X3F);

    Write_Command(0XAB);            //Set VDD regulator
    Write_Command(0X01);            //Regulator Enable

    Write_Command(0XAD);            //External /Internal IREF Selection
    Write_Command(0X8E);

    Write_Command(0XB1);            //Set Phase Length
    Write_Command(0X22);

    Write_Command(0XB3);            //Display Clock Divider
    Write_Command(0XA0);

    Write_Command(0XB6);            //Set Second precharge Period
    Write_Command(0X04);

    Write_Command(0XB9);            //Set Linear LUT

    Write_Command(0XBC);            //Set pre-charge voltage level
```

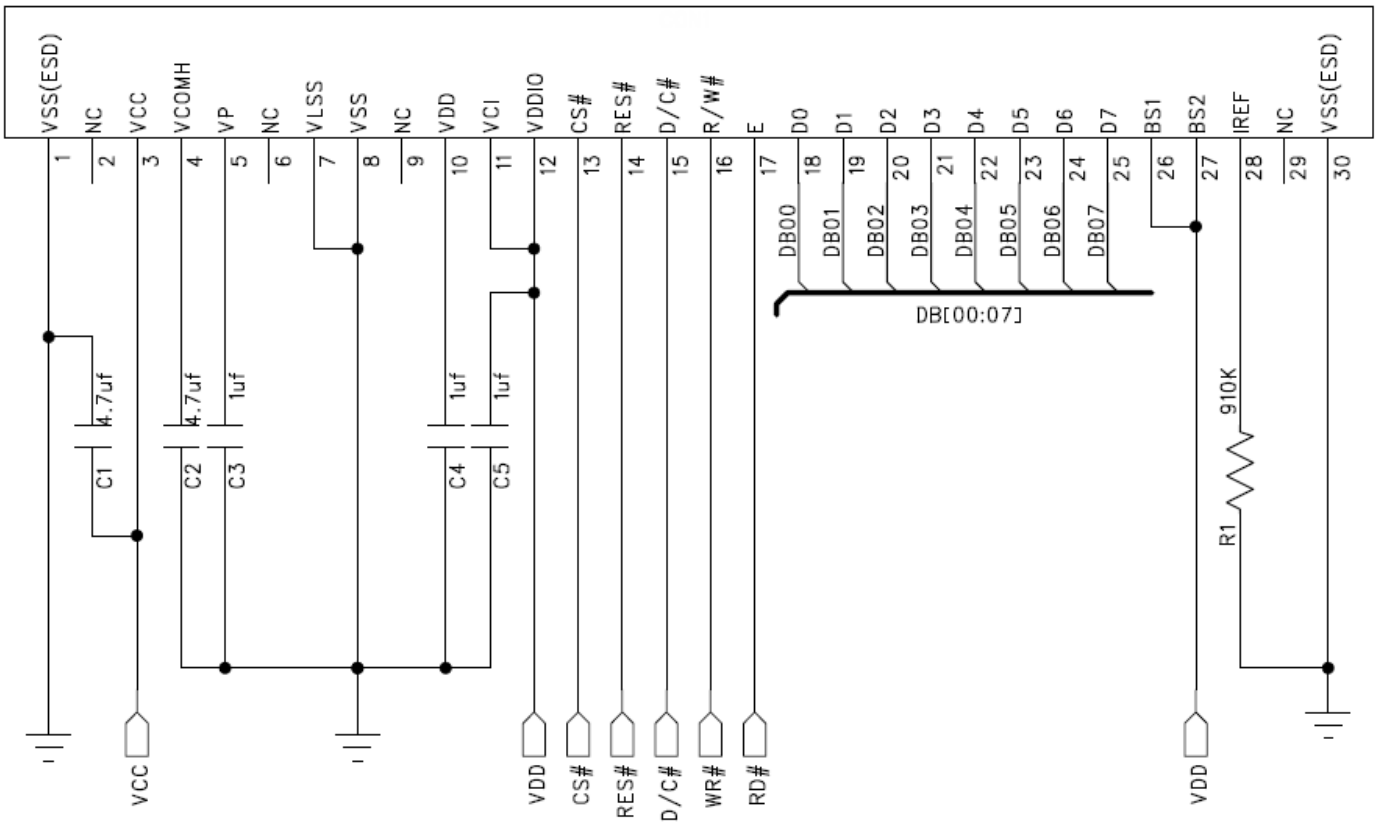
```
    Write_Command(0X10);          //0.5*VCC

    Write_Command(0XBD);          //Pre-charge voltage capacitor Selection
    Write_Command(0X01);

    Write_Command(0XBE);          //Set COM deselect voltage level
    Write_Command(0X07);          //0.82*VCC

    Write_Command(0XAF);          //Display ON

}
```

■ SCHEMATIC EXAMPLE

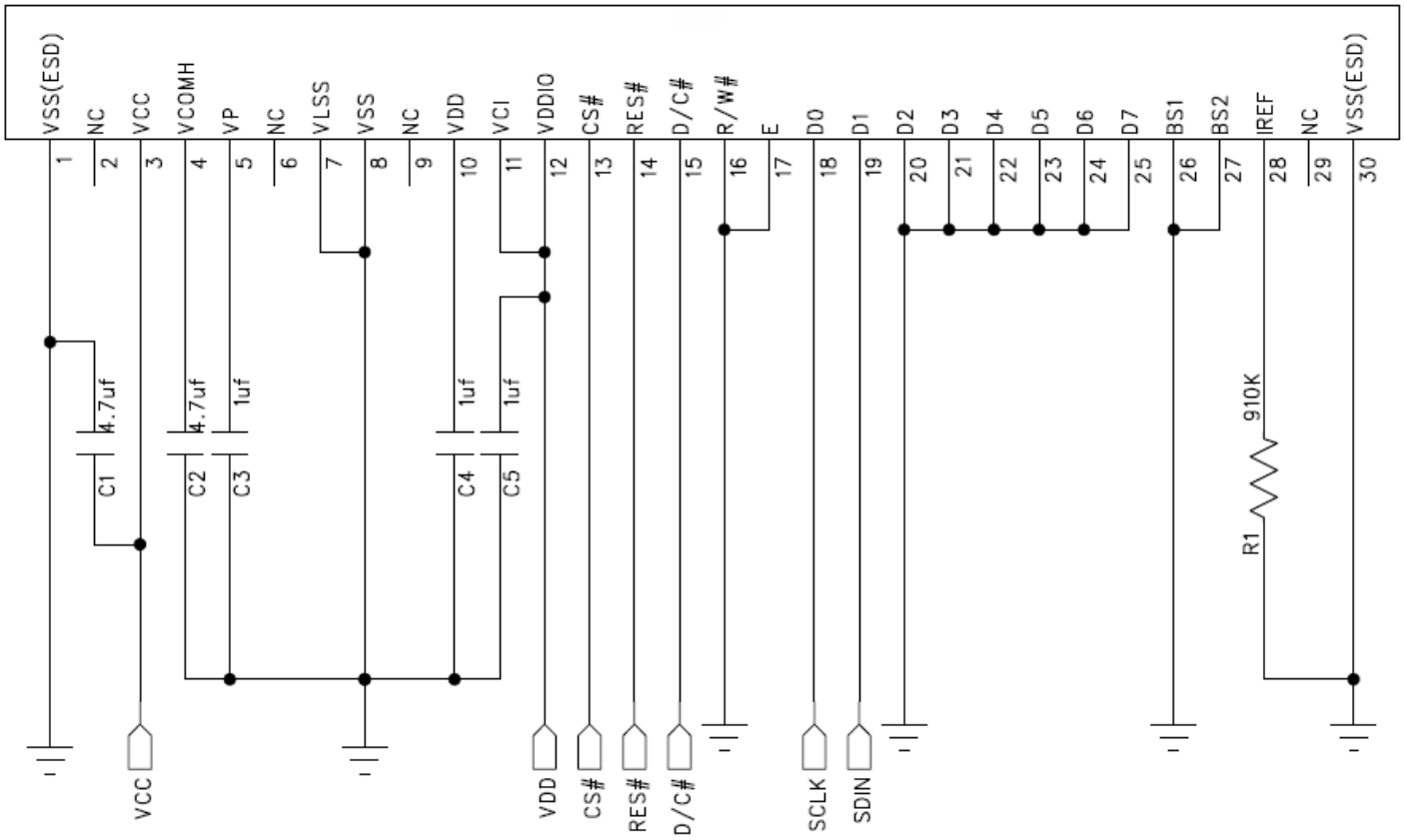
◆ 6800-Series MCU Parallel Interface Application Circuit:



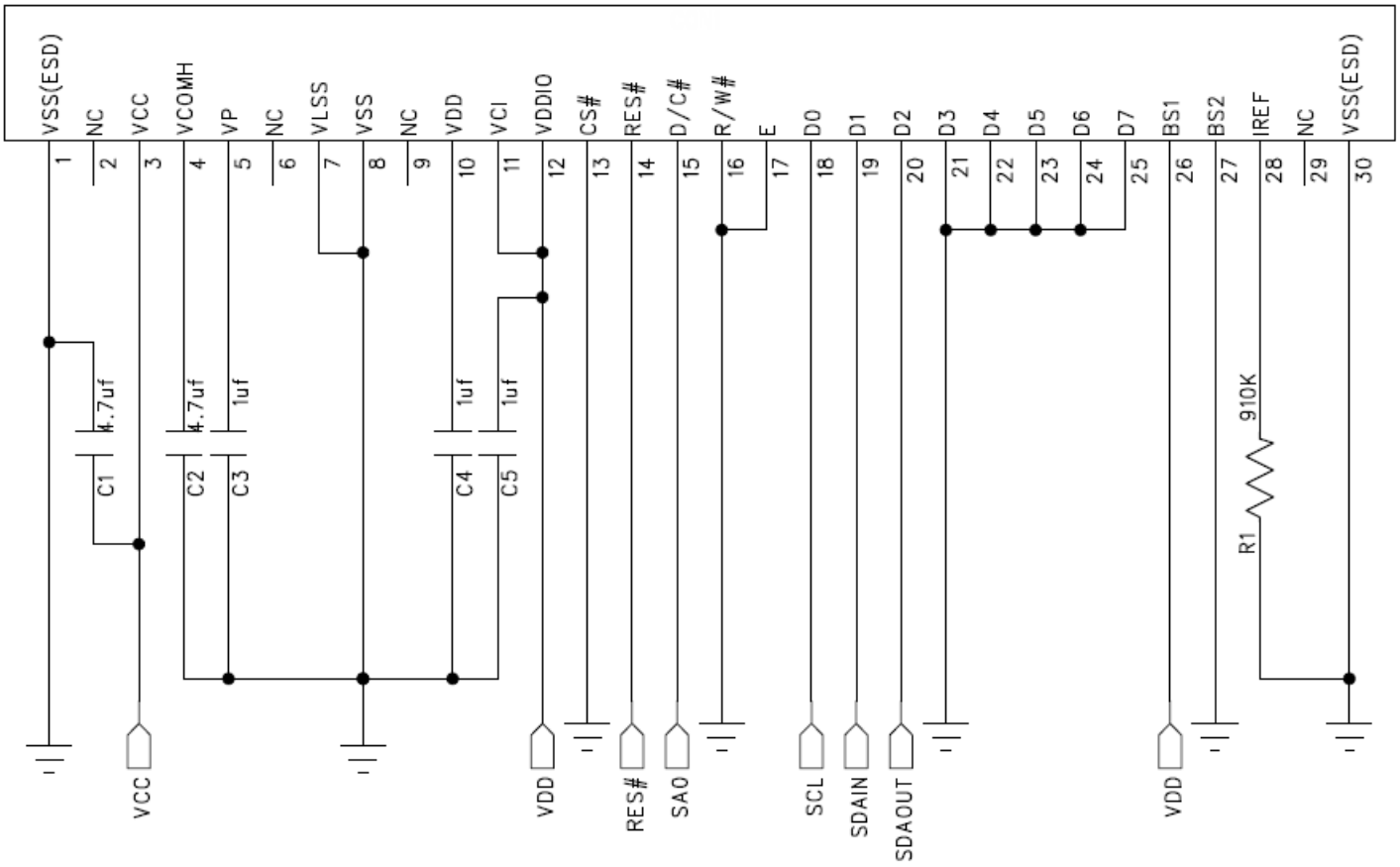
◆ 8080-Series MCU Parallel Interface Application Circuit:



◆ 4-wire SPI Serial Interface Application Circuit:



◆ IIC Interface Application Circuit:



For Above Circuits:

VCC and VDD are supplied by external power, VCC = 12.0V, VDD=3.0V;

C1~C2: 4.7uF/35V+/-10% tantalum capacitor (suggest), C3~ C5:1uf;

R1=910 KΩ.

Note:

The value of components is recommended value. Select appropriate value against module application.

■ RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		85±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		80±2℃, 96 hours	
Low Temperature Storage (LTS)		-40±2℃, 200 hours	
Low Temperature Operating (LTO)		-30±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

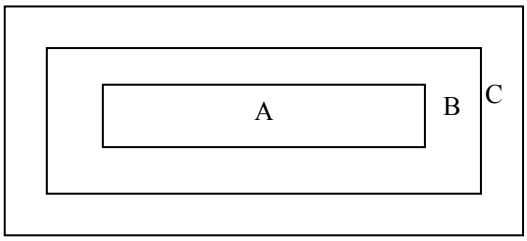
■ OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

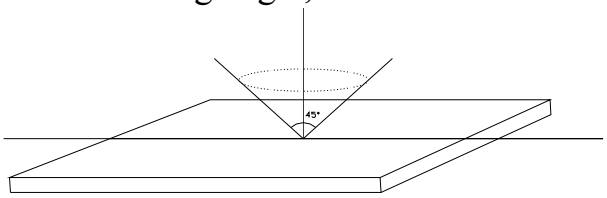
1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area
Zone B: Viewing Area except Zone A
Zone C: Outside Viewing Area
Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

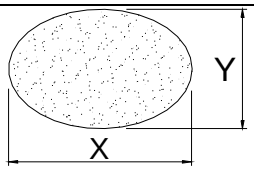
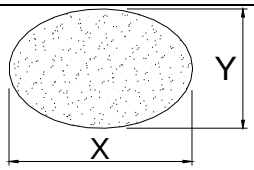
◆Inspection Criteria

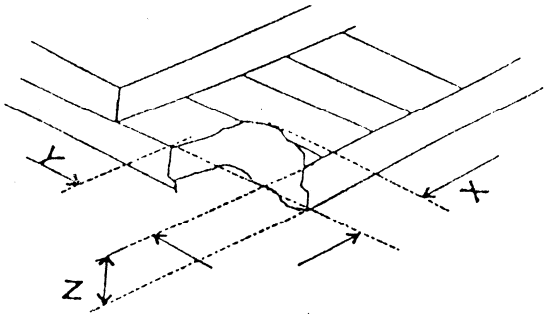
1 Major defect : AQL= 0.65

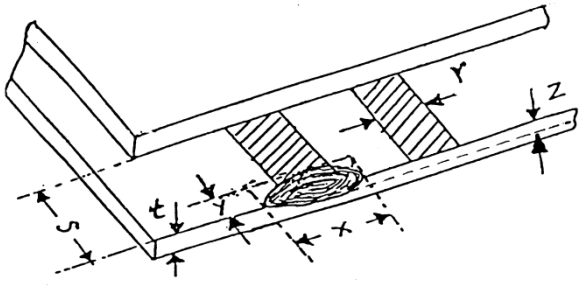
Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

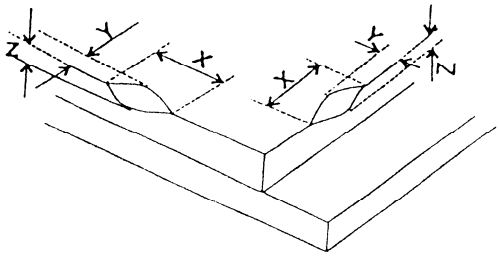
2 Minor Defect : AQL= 1.5

Item	Criterion	
	Size (mm)	Accepted Qty

<table>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4"> 
</td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td>0.15＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4"> 
</td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
(mm)
 

<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
(mm)
 

<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
(mm)
 

<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module cannot be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For TRULY standard products, we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.